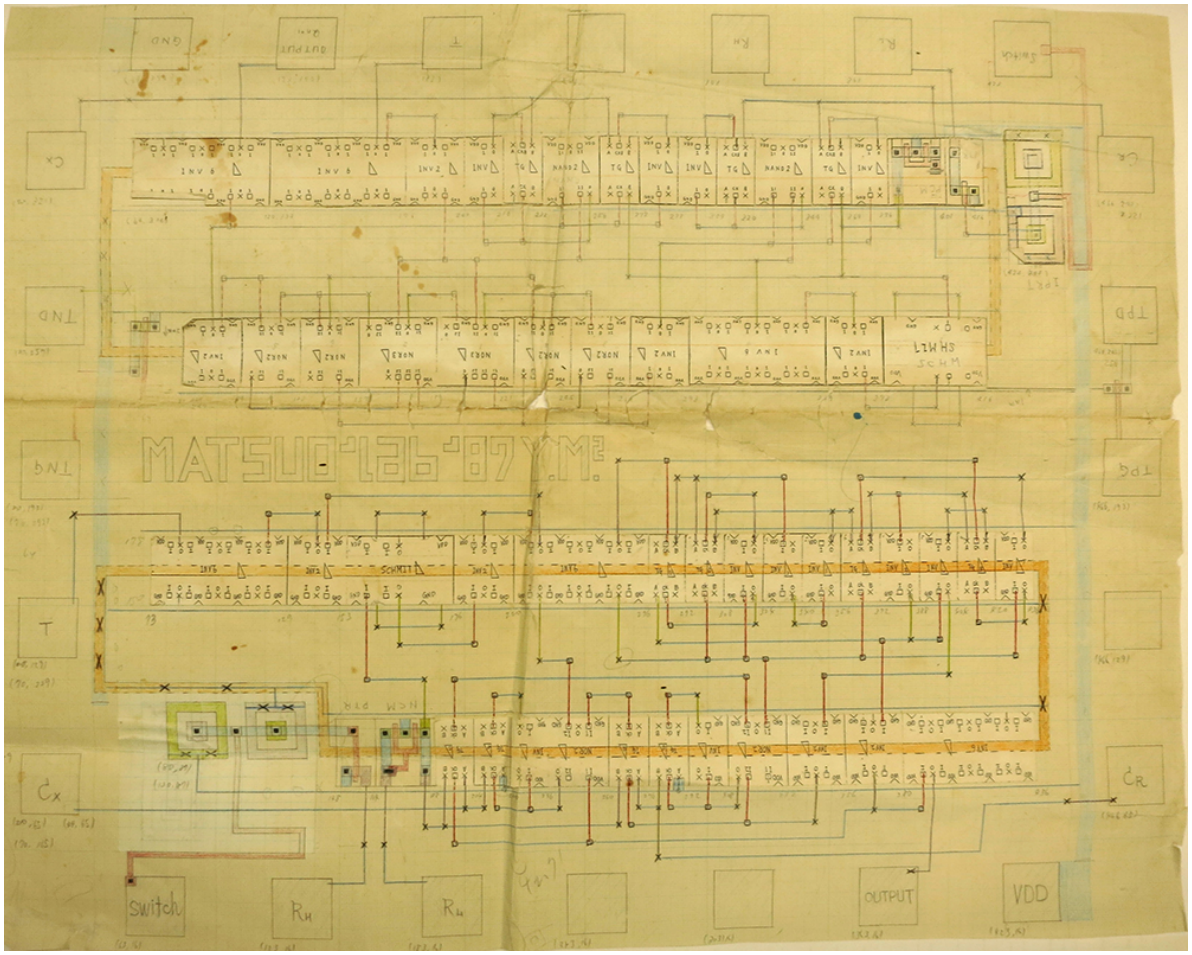
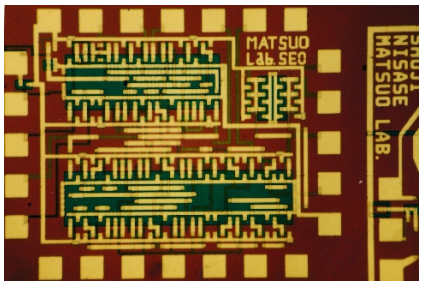
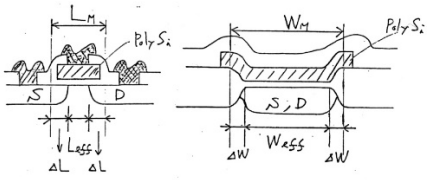
2 Design (2) layout







$L_{eff} = L_M - 2\Delta L$ $\quad W_{eff} = W_M - 2\Delta W$

Parameter		Size nMOS	Size pMOS	Unit
Threshold voltage V_T		1.0	-1.2	V
Mobility (maximum) μ_{eff}		373	149	$cm^2V^{-1}sec^{-1}$
Substrate bias effect γ		1.4	0.41	$V^{\frac{1}{2}}$
Channel length modulation λ	L=5μm	0.056	0.13	V^{-1}
	L=10μm	0.012	0.022	V^{-1}
ΔL		1.83	1.7	μm
ΔW		2.64	2.14	μm
Junction depth of S,D X_j		2.3	2.1	μm
Gate oxide thickness T_{ox}		720	720	Å

Measured SPICE parameter for SPICE simulation
(p-well dose $8X10^{12}$ atoms/cm^2)