1 Design (1) CAD

Design and fabrication of CMOS IC using equipment made in-house
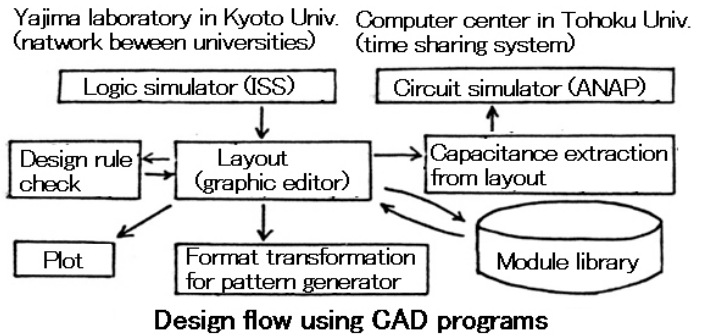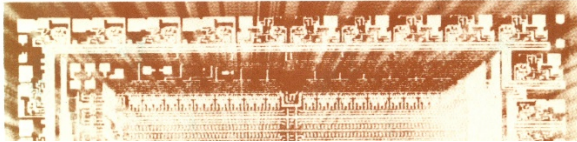

半導体工学シリーズ ❼

半導体集積回路設計の基礎

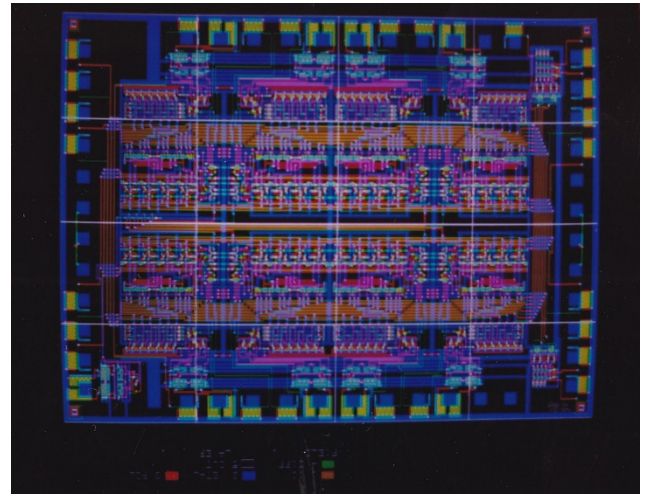西澤潤一編　江刺正喜著

培風館

1986年

Text book in Japanese "Basics of integrated circuit design" M.Esashi (1986) Baifukan

Yajima laboratory in Kyoto Univ. (natwork beween universities)　Computer center in Tohoku Univ. (time sharing system)

Logic simulator (ISS)　Circuit simulator (ANAP)

Design rule check ← Layout (graphic editor) → Capacitance extraction from layout

Plot　Format transformation for pattern generator　Module library
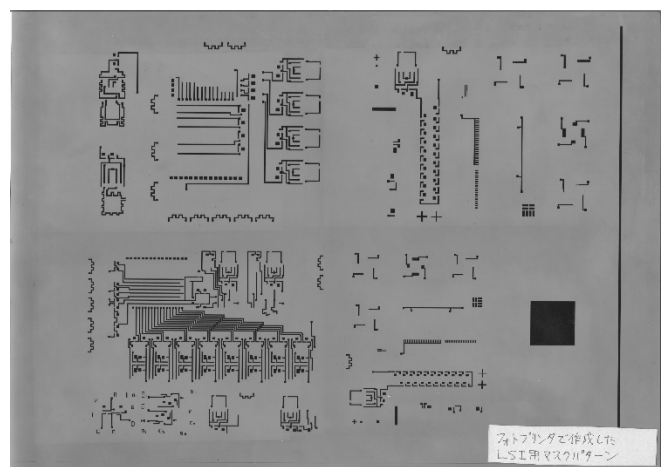
Design flow using CAD programs

Graphic display connected to LSI11 (DEC) for LSI design

Layout editor programed by M. Esashi using Fortran

Photo-printer for printing out the layout pattern

Mask negative printed out on a transparent film

(M. Esashi : Prototyping and Education of LSI in University, J. of the IECE, 68, 1 (1985) 50－52) (in Japanese)

(M. Esashi, A. Komatsu, M. Asibe, M, Ohtomo : Design/Fabrication System for Custom LSI (1) (Overview of the System), (2) (Design Environment), (3) (NMOS process and Evaluation), S58 Convention of the IECE, 401-3 (1983)) (in Japanese)

(M. Esashi, A. Masuda, T. Matsuo : CAD System for LSI Design, Joint Convention of Electrical Academic Societies in Tohoku Region, 2D21 (1984))(in Japanese)