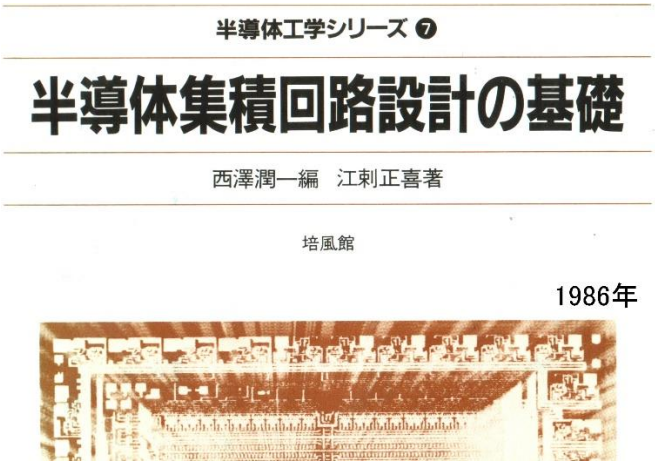
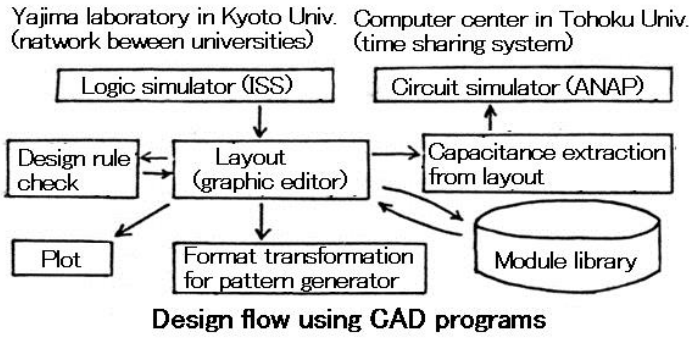
Design and fabrication of CMOS IC using equipment made-in-house

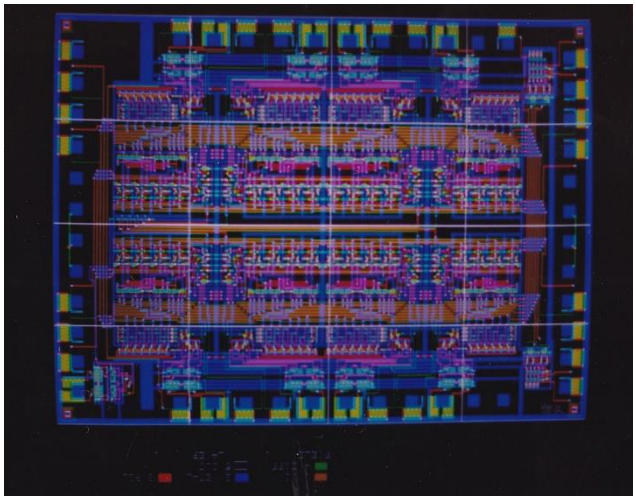
[1] Design





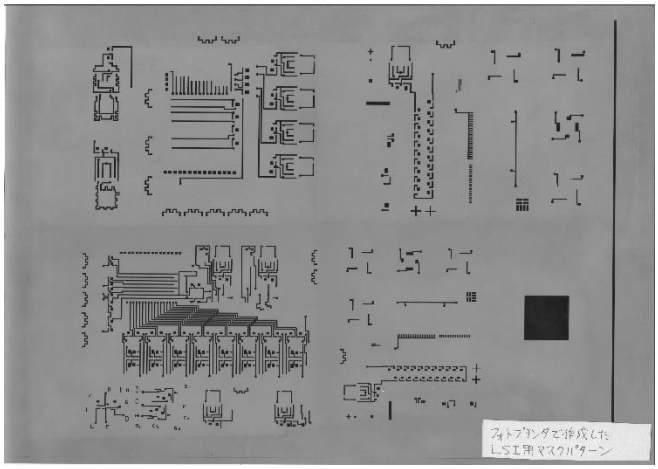
Text book in Japanese “Basics of integrated circuit design” M.Esashi (1986) Baifukan

Graphic display connected to LSI11 (DEC) for LSI design



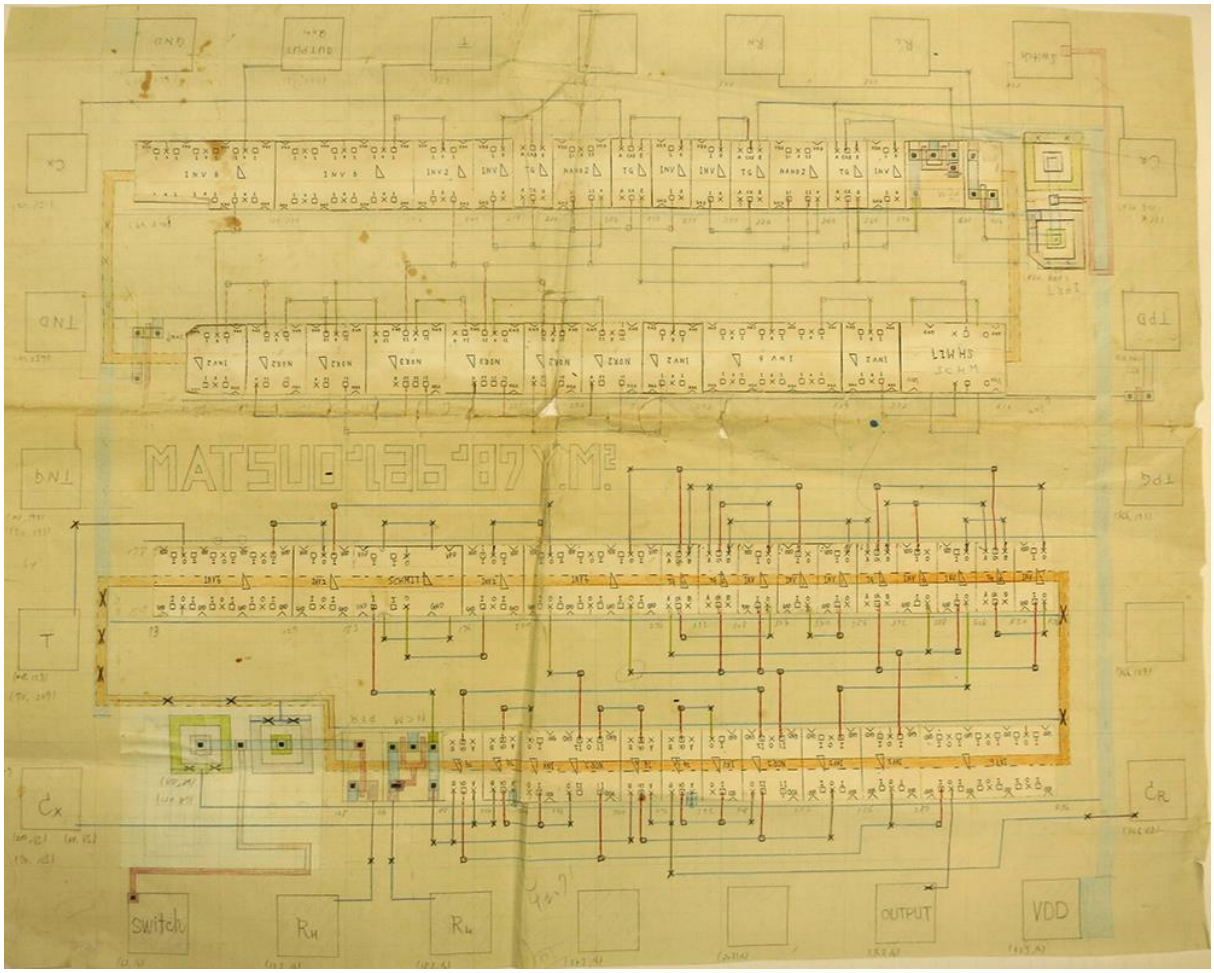
Layout editor programed by M. Esashi using Fortran

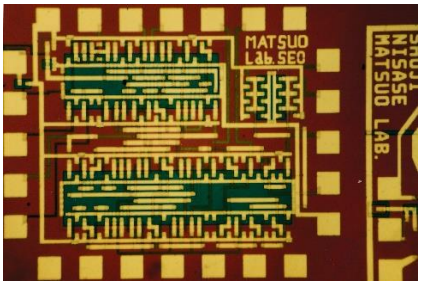
Photo-printer for printing out the layout pattern

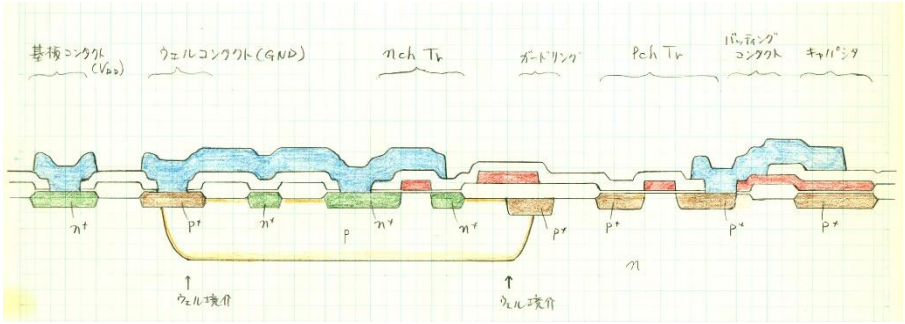


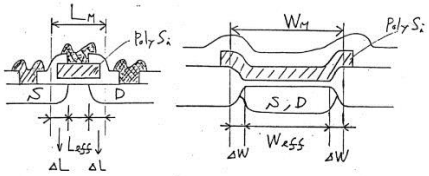
Mask negative printed out on a transparent film

(M. Esashi : Prototyping and Education of LSI in University, J. of the IECE, 68, 1 (1985)50－52) (in Japanese)
(M. Esashi, A. Komatsu, M. Asibe, M, Ohtomo : Design/Fabrication System for Custom LSI (1) (Overview of the System), (2) (Design Environment), (3) (NMOS process and Evaluation), S58 Convention of the IECE, 401-3 (1983)) (in Japanese)
(M. Esashi, A. Masuda, T. Matsuo : CAD System for LSI Design, Joint Convention of Electrical Academic Societies in Tohoku Region, 2D21 (1984))(in Japanese)









$L_{eff} = L_M - 2\Delta L$ $\quad W_{eff} = W_M - 2\Delta W$

Parameter		Size nMOS	Size pMOS	Unit
Threshold voltage V_T		1.0	-1.2	V
Mobility (maximum) μ_{eff}		373	149	$cm^2V^{-1}sec^{-1}$
Substrate bias effect γ		1.4	0.41	$V^{\frac{1}{2}}$
Channel length modulation λ	L=5μm	0.056	0.13	V^{-1}
	L=10μm	0.012	0.022	V^{-1}
ΔL		1.83	1.7	μm
ΔW		2.64	2.14	μm
Junction depth of S,D X_j		2.3	2.1	μm
Gate oxide thickness T_{ox}		720	720	Å

Measured SPICE parameter for SPICE simulation
(p-well dose $8X10^{12}$ atoms/cm^2)