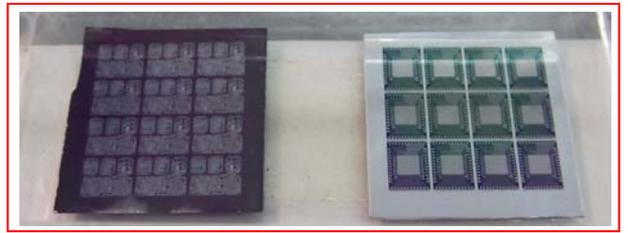
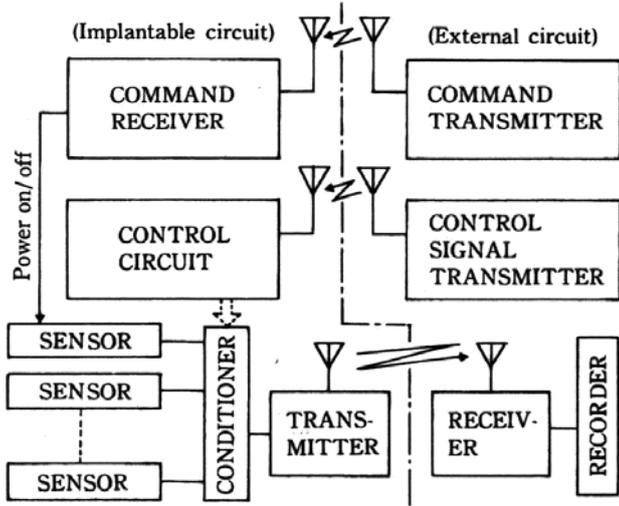
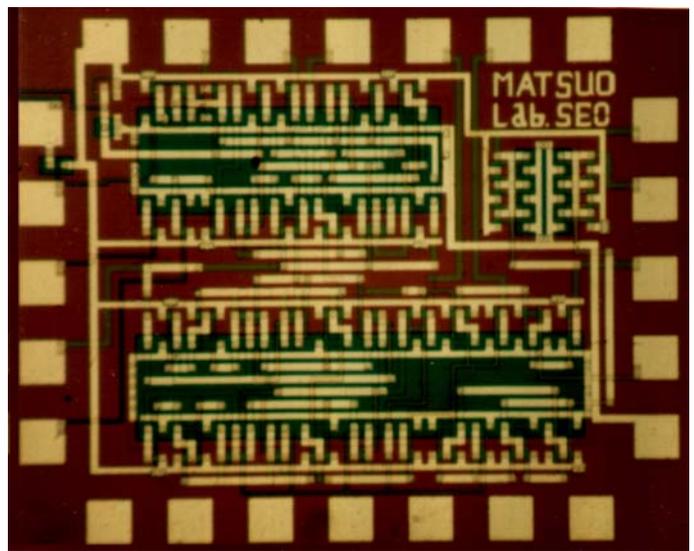
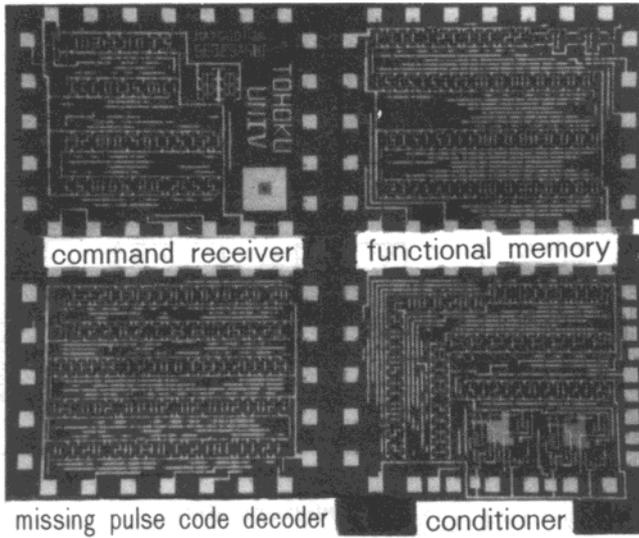
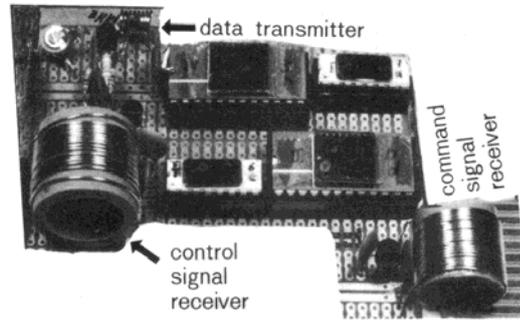


カスタム集積回路

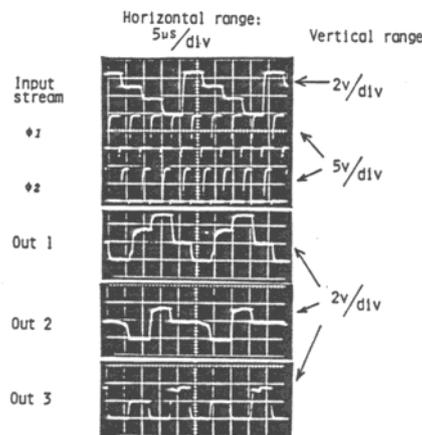
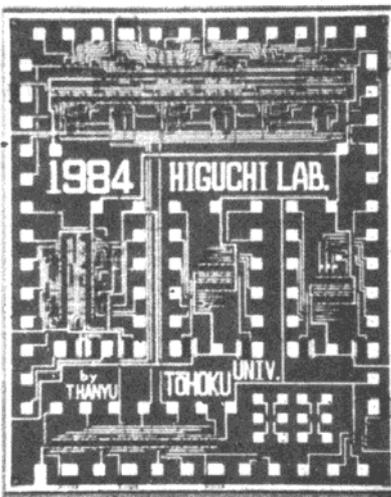


体内テレメータ CMOS 回路 バレルシフト用 NMOS 回路



体内テレメータ用 CMOS 集積回路

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多値論理集積回路



参考文献 : M.Kameyama, T.Haniyu, M.Esashi and T.Higuchi, An NMOS Pipelined Image Processor Using Quaternary Logic, IEEE Int.Solid-State Circuit Conf.,WPM8.2 (1985) pp.86-87

自作装置による CMOSLSI の設計試作に関しては、3F「試作装置展示室」参照