

# ISIM2011

International Symposium on Integrated Microsystems

## High Efficiency Integrated MEMS Production Technology

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# First Program: **Microsystem Integration Project**

**Prof. Esashi, Tohoku Univ**

**Dr. Maeda, AIST**

**High Efficiency  
Integrated MEMS  
Production**

•Size-free Integration  
MEMS fabrication by  
micro-forming



**AIST UMEMSME RC**

**Heterogeneous Integration**  
MEMS, LSI, RF, Analog, Power  
Optic, Bio, Fluidic, Chemical, etc.  
Si, III-V, Piezo, etc.

High value added devices

**Production Stage  
Prototyping (8 inch)**

Healthy aging (Artificial sensing organ)  
Safety and security (Sensor network)  
Advanced IT (Multi band wireless, etc.)

**Massive Parallel  
EB Lithography**

Maskless lithography  
for small batch

**Hands on Access  
to Fab. Facilities**

Low cost &  
low risk R&D

**Initial Stage  
Prototyping (20mm□)**

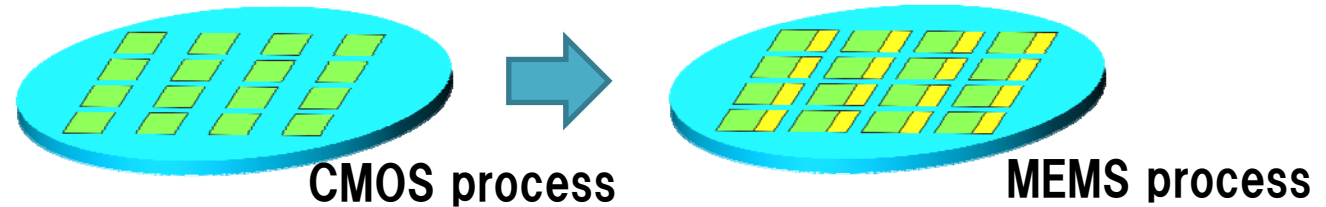
**Tohoku Univ.**

# High Efficiency Integrated MEMS Production Technology

- Improvement of Heterogeneous Integration Process
  - Size-free Integration
    - Bonding Technology
    - High-precision, High-speed, Batch Assembly Technology
    - Optimization of each Device Process
  - Large Wafer TSV Interposer
    - Large Wafer DRIE Process, TSV Formation Process
- High Efficiency Production using Forming Process
  - Wiring Pattern Fabrication by Imprint Process
  - MEMS Fabrication by Micro-forming
    - MEMS Fabrication using Injection Molding

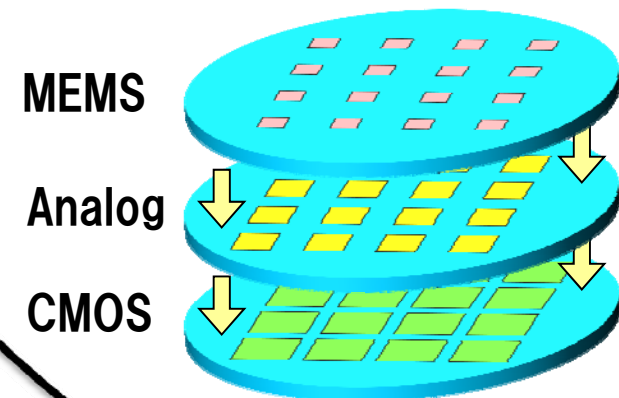
# Heterogeneous Integration Process

**SoC type (System on Chip)**



**SiP type (System in Package)**

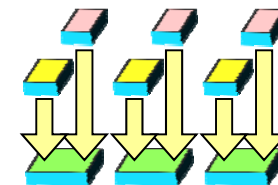
**Wafer-to-Wafer (W2W, WLP)**



**Chip-to-Wafer (C2W)**



**Chip-to-Chip (C2C)**



# Applications of Integration Processes

- **SoC type**
  - High speed, Small signal (Low noise)
  - Mass production devices (High R&D cost)
- **WLP type**
  - MEMS protection by cap-wafer
  - Incompatible MEMS & MOS process
  - 3D Integration
- **SiP type**
  - Nonidentical chip size and wafer size
  - Small batch, Quick commercialization

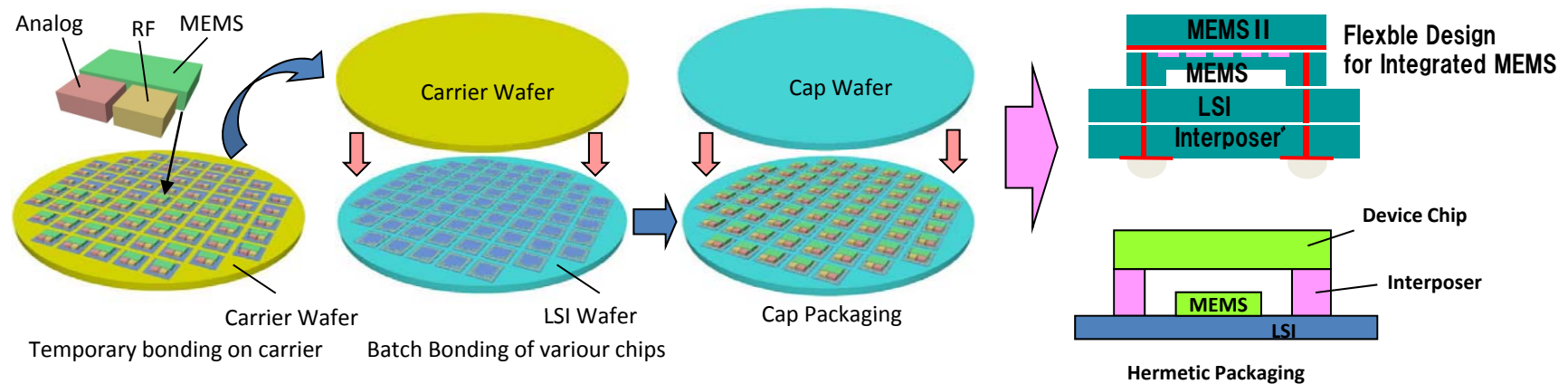
# Comparison of Integration Processes

	SoC	WLP	SiP
Assembly Cost	◎	○	×
Data Rate	◎	○	△
Power Consumption	◎	○	?
Process Flexibility	×	○	◎
Wafer Size Flexibility	?	×	◎
Device Performance	?	○	◎
Chip Size Flexibility	?	×	◎
System Performance	?	?	?
Total Cost	?	?	?



# (Wafer & Chip) Size-Free Integration

## Wafer-scale integration for a variety of chips



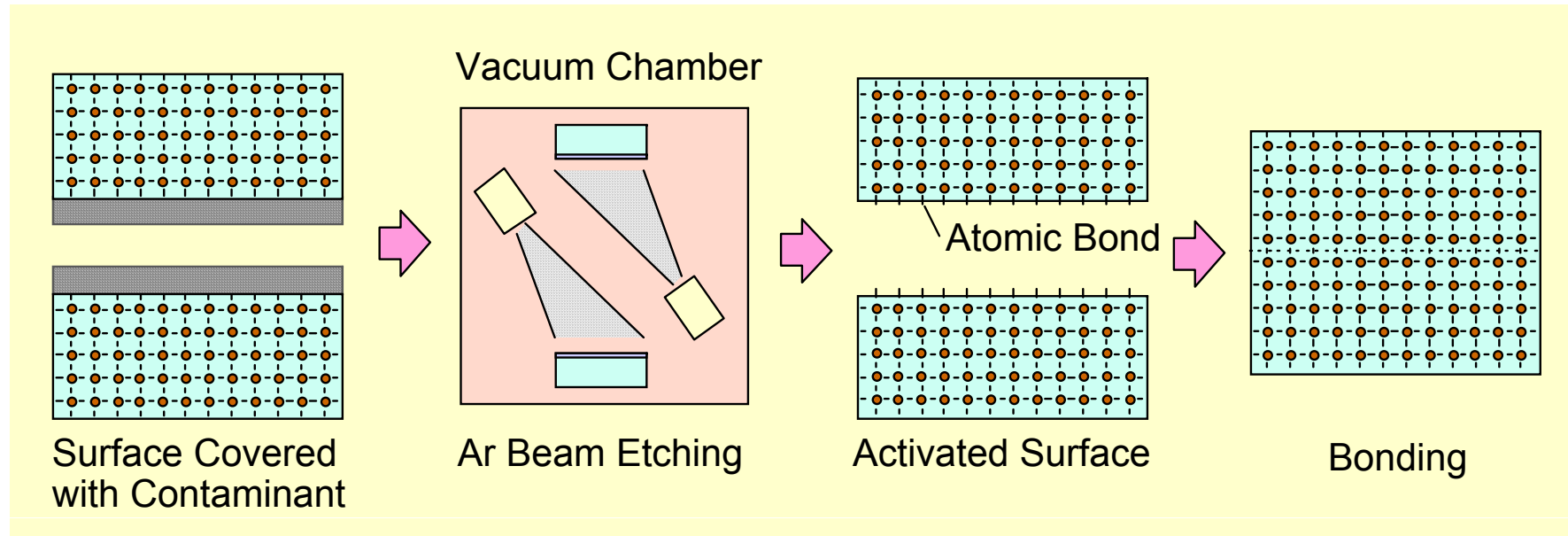
## Merits

- Device design free from the limitations of wafer size and/or chip size.
- Optimization of device fabrication process of MEMS, LSI, Analog, etc.
- Multi-layer stacking, packaging, and hermetic sealing using TSV Interposer.

## Technologies

- Temporary bonding and de-bonding.
- High speed sorting of chips on a carrier wafer.
- Low-damage and low temperature bonding process.

# Room-temperature Bonding by Ar Beam and Bonding in Vacuum



Making Unstable Surface State by Ar-beam Etching in Vacuum  
↓ (Surface Activation)

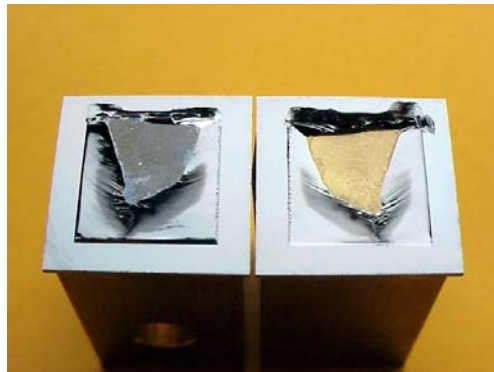
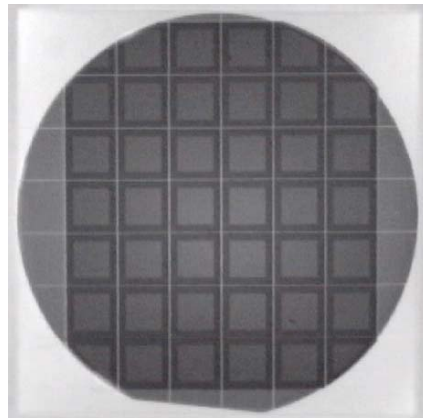
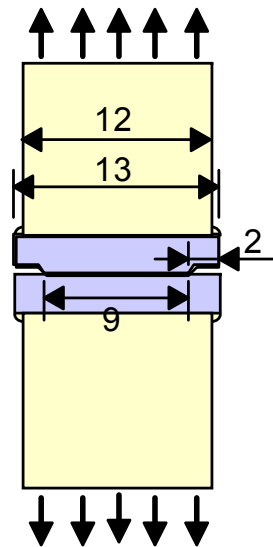
**Room-temperature Bonding**

**Surface Activated Bonding (SAB)**

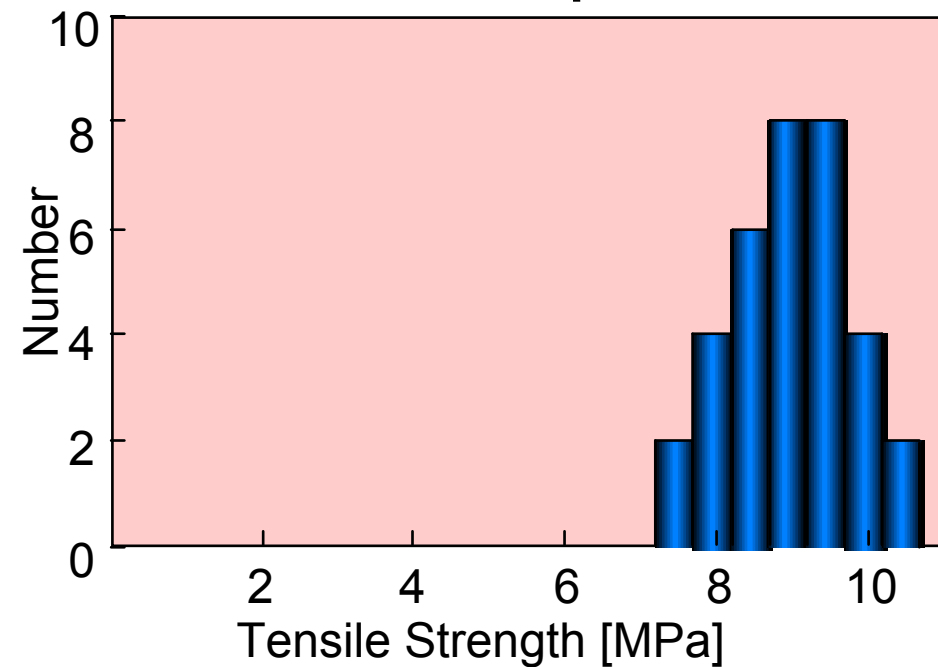


# Bonding Strength Evaluation by Tensile Test

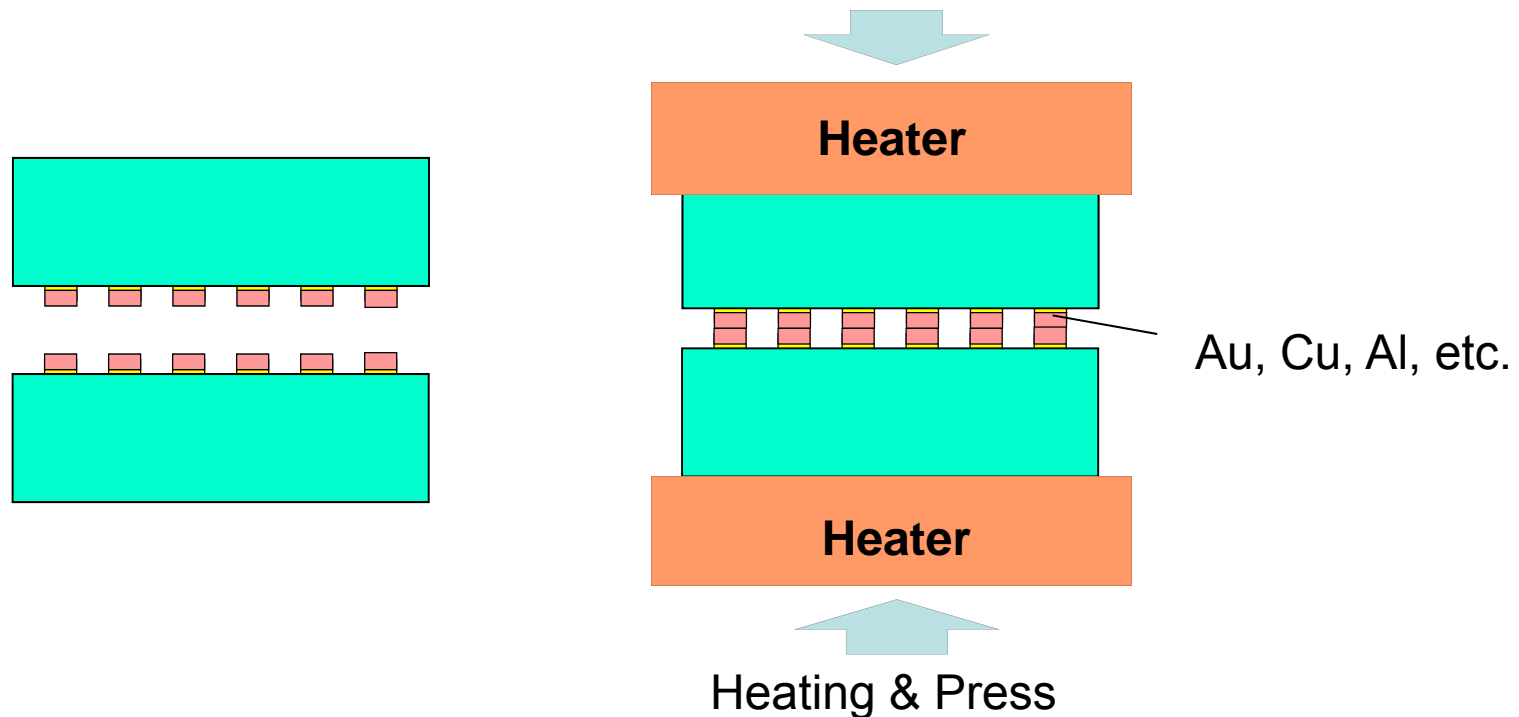
## Specimen



## Distribution of tensile strength of the 34 specimens cut from a bonded wafer pair



# Thermo Compression Bonding of Metals



Process Temperature 200°C~

Mechanical bonding and electric connection, simultaneously  
High reliability and hermeticity of metal direct bonding

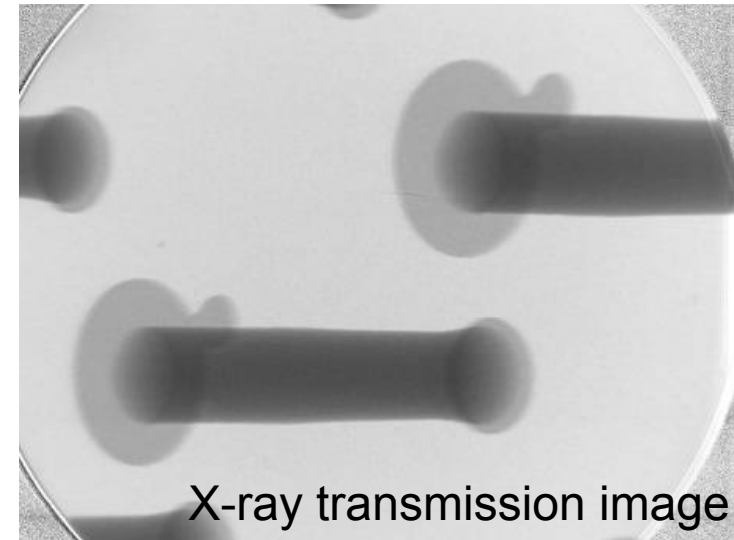
# Large Wafer TSV Interposer

## TSV fabrication in 300 mm Si wafers

State-of-the-art CMOS Devices  
Fabricated by 300 mm Process



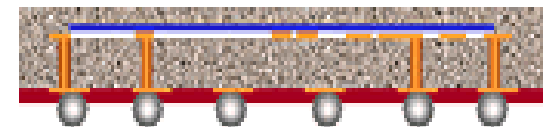
Heterogeneous Integration  
using 300mmTSV



System in Package



3D Stacked LSI



MEMS Package

# 300 mm DRIE Apparatus

Sumitomo Precision  
Products Co.  
Pegasus300



10um Via, 70min etching

	Center	Right
全体図		
エッチ深さ	208.7um	215.4um
エッチレート	3.0um/min.	3.1um/min.
	Center	Right
上部拡大図		
下部拡大図		
側壁角度	89.8°	89.8°
側壁荒さ	48nm	48nm
PR選択比	24	25

100nm trench, 3min etching

パターン中央
2.5um
0.8um/min.
パターン中央
89.8°
~8nm
9

# Automatic Coater and Developer

200, 300mm wafers compatible

Fully automatic

Two type photoresists

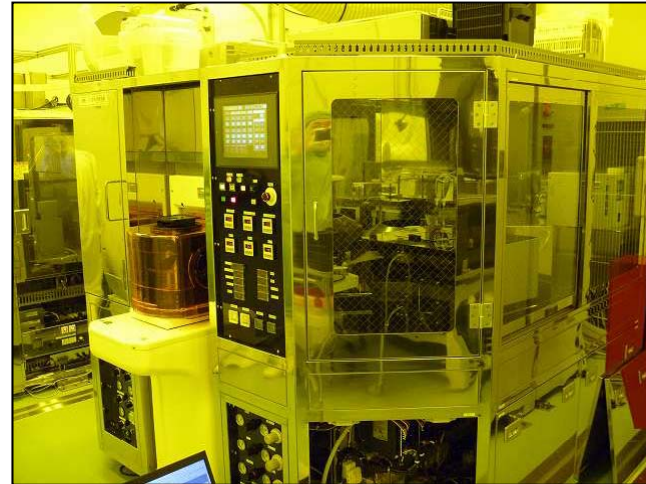
Resist 1: 0.8-1.5  $\mu\text{m}$

Resist 2: 10.0-20.0  $\mu\text{m}$

Primer

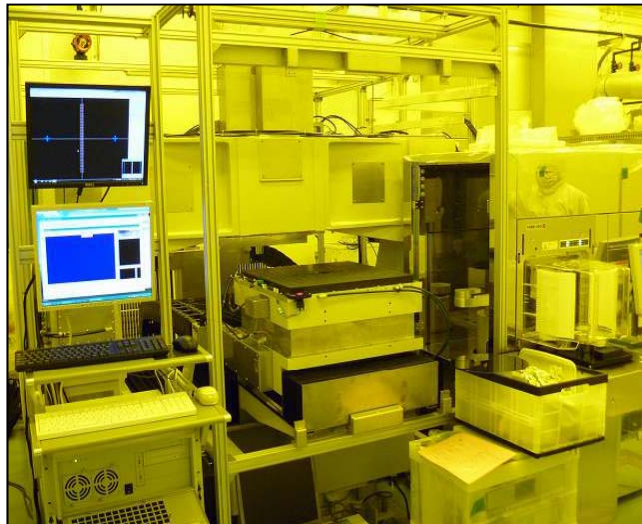
3 Hot plates

1 Cool plate



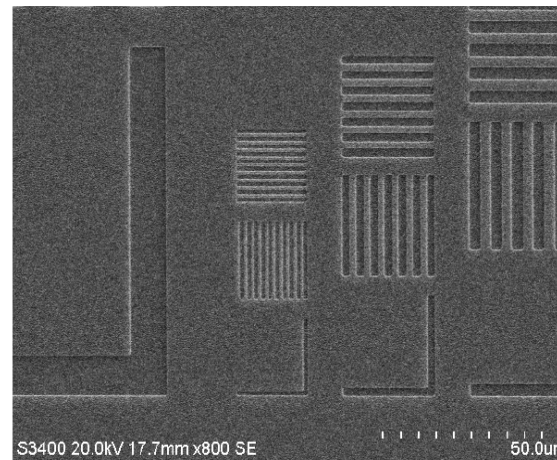


# Mask-less Lithography

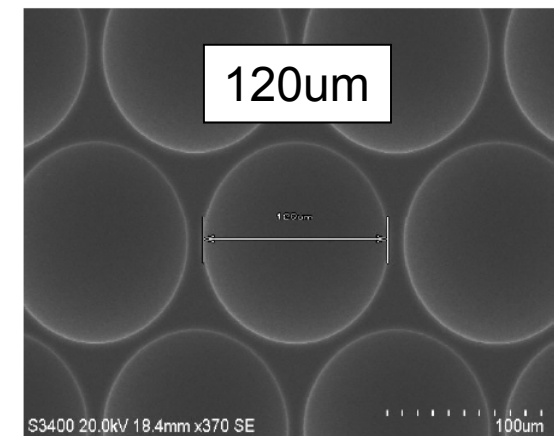
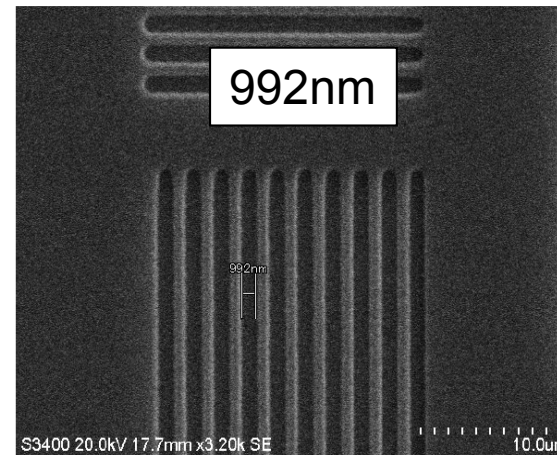
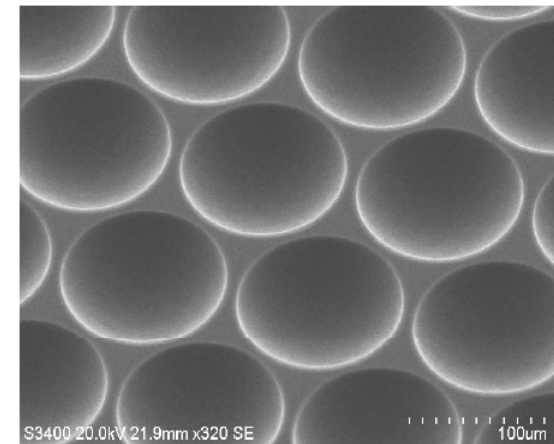


500x500 mm Litho-Area  
DMD projection  
Step and repeat or Scan  
Thick resist >100μm

L&S Pattern

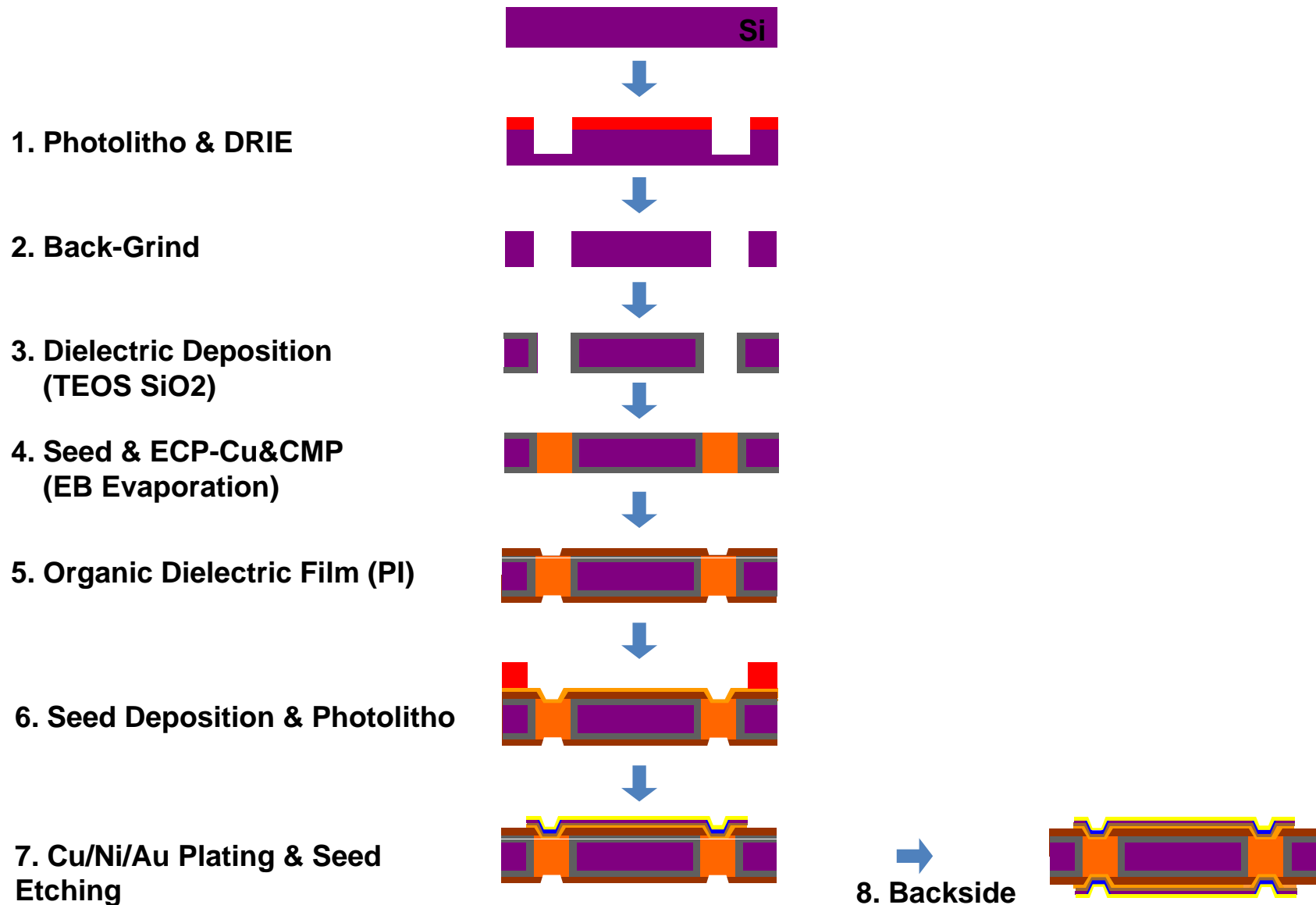


Gray-scale lithography



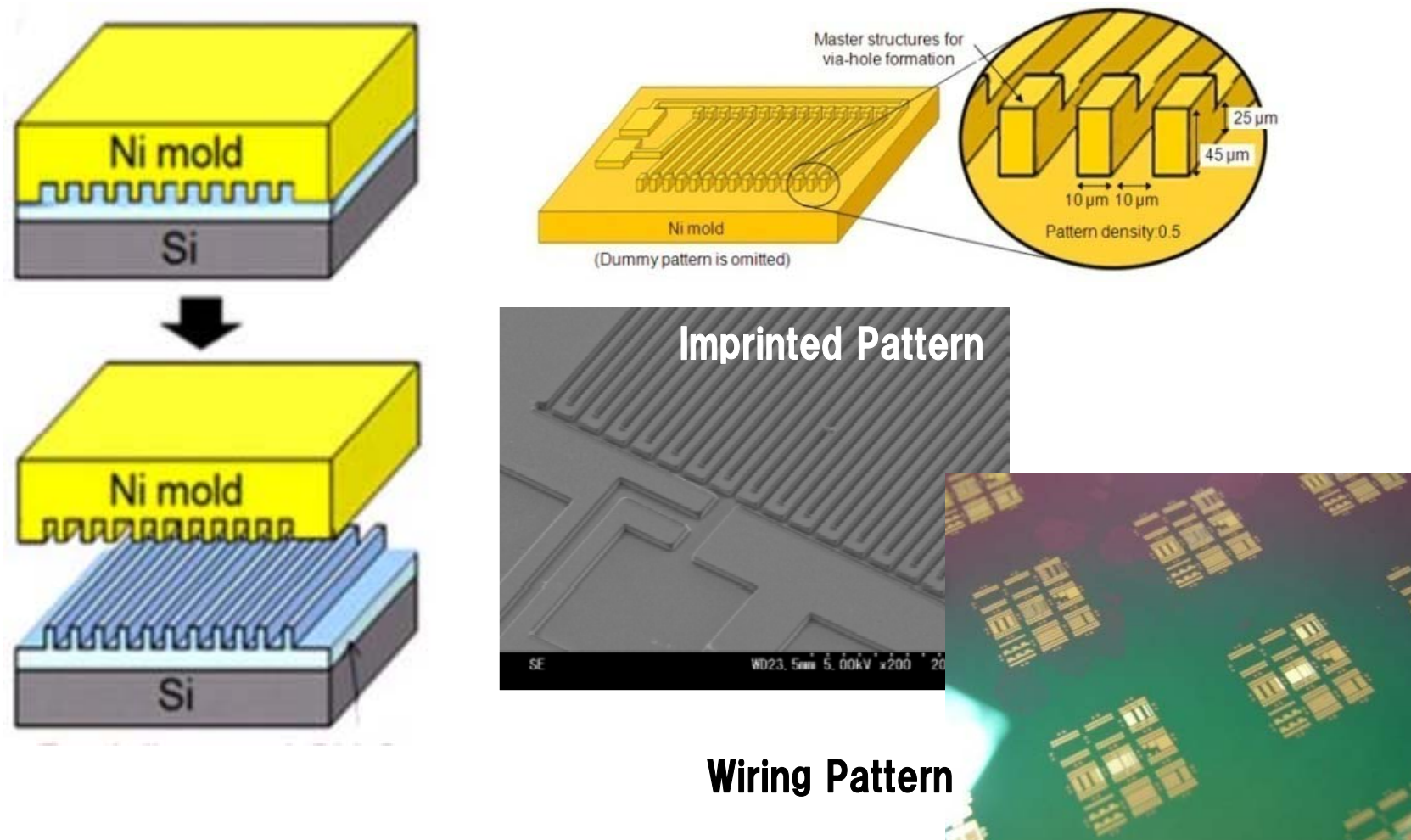


## ➤ 300mm TSV Interposer Process Flow (Via First)

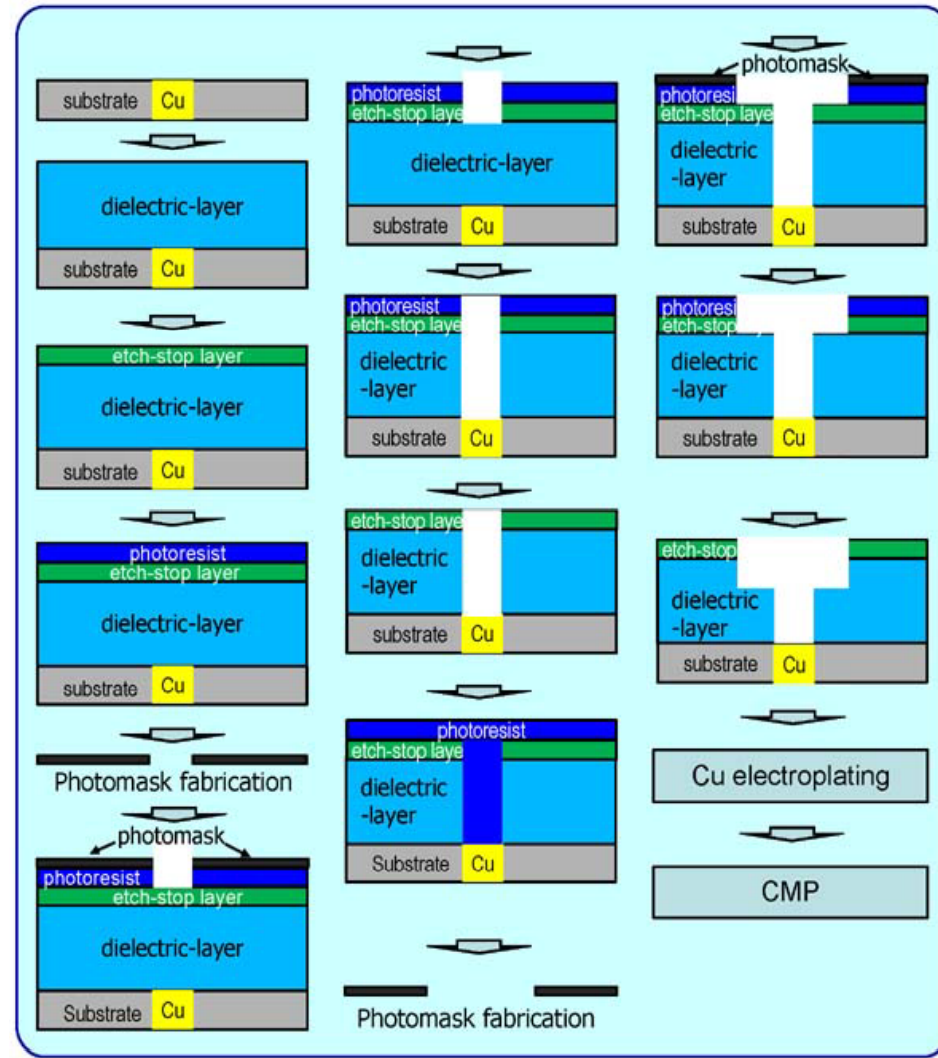


# Large Wafer TSV Interposer

## Wiring pattern fabrication by imprint process

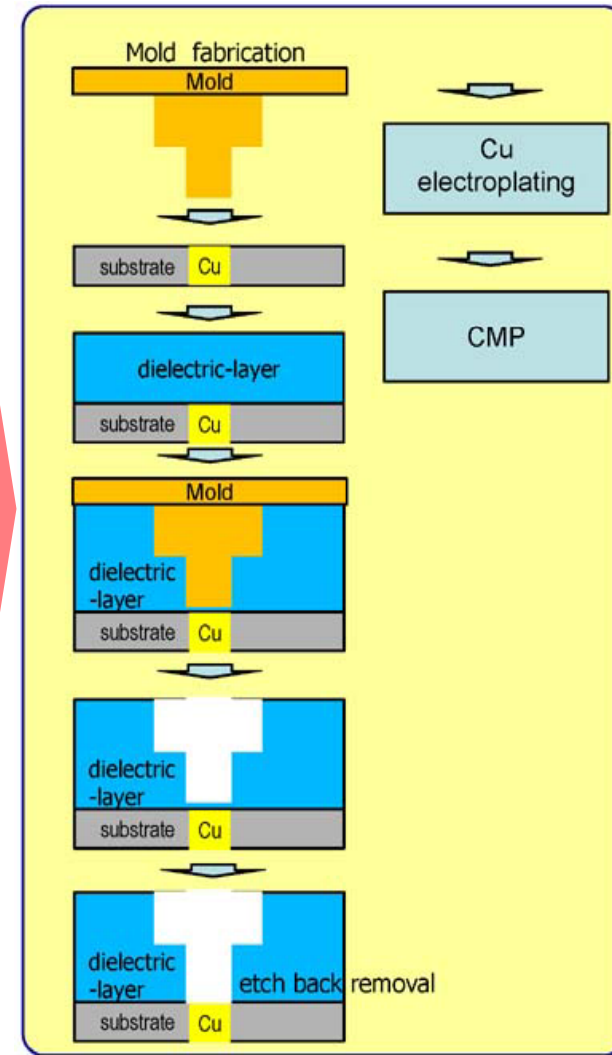


# Simple wiring process by imprint lithography



(a) Photo-lithography

Process Simplification

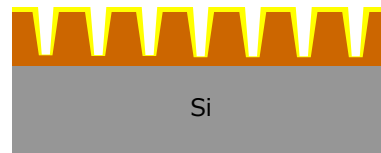


(b) Imprint Lithography

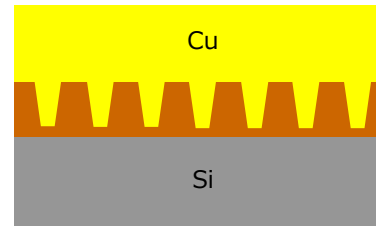
# Cu Wiring Pattern Formation by Electroplating and Polishing



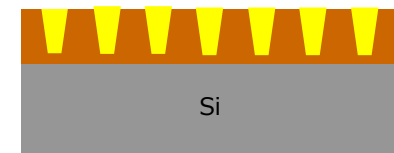
(a) Pattern formation by imprint



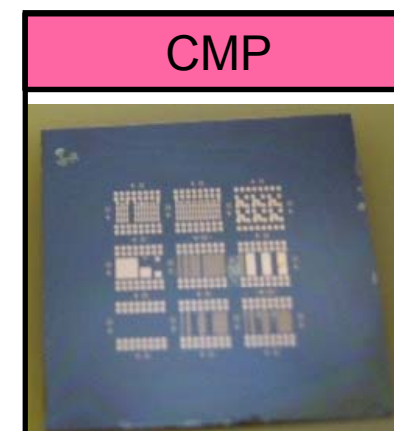
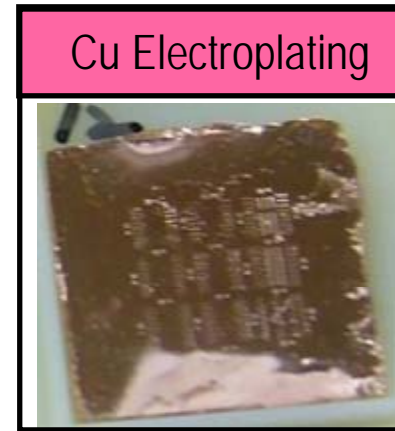
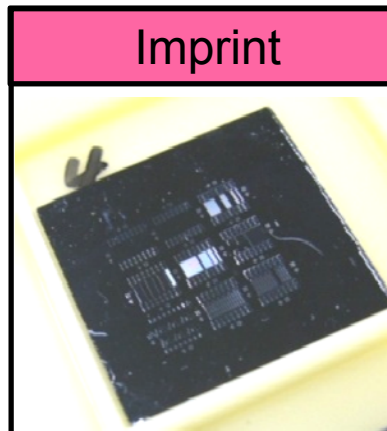
(b) Seed and barrier deposition



(c) Cu electroplating



(d) Polishing



# MEMS Fabrication by Micro-forming

## MEMS fabrication using injection molding

**Low Cost MEMS  
Production**



**Large Wafer Process  
→ 8 inch line**



**New Concepts for Low Cost MEMS Process**



**MEMS Fabrication by Micro-forming → Injection Molding**



**Low Initial Cost: Molding-machine and Mold, only  
No Vacuum Process: High Throughput**



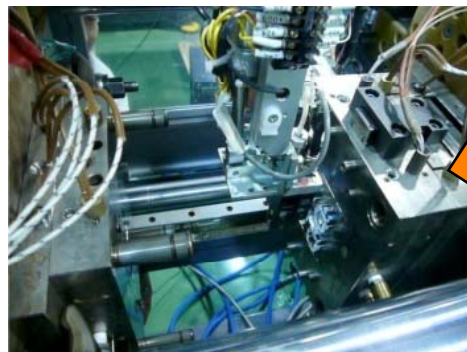
**New Application by Low-cost Polymer MEMS**



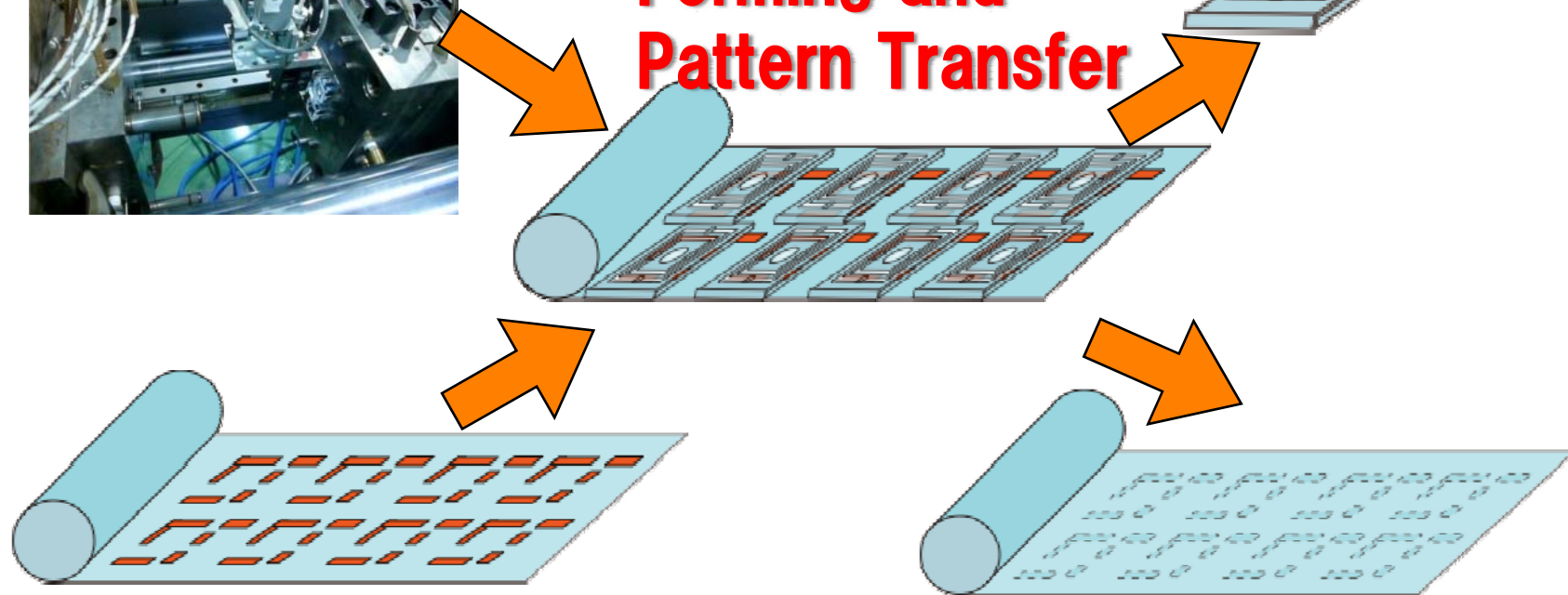
# MEMS Fabrication by Micro-forming

Mold with membrane for MEMS

MEMS device



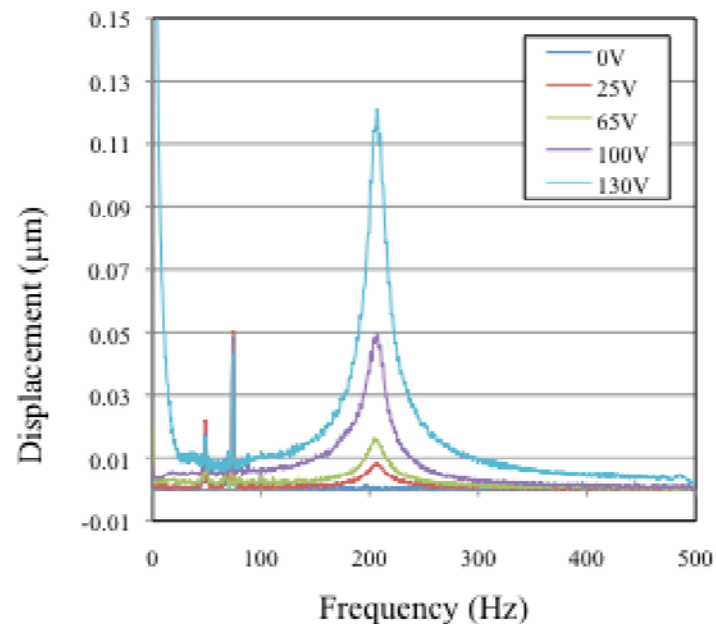
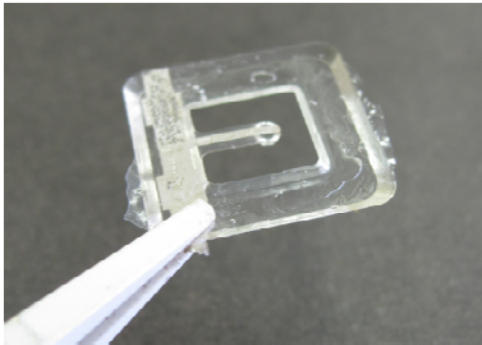
**Forming and  
Pattern Transfer**



Sheet with printed wiring patterns



# Prototype Device by Forming and Printed Pattern Transfer



1) Printed Wiring and Functional Material



2) UV Resin Filling



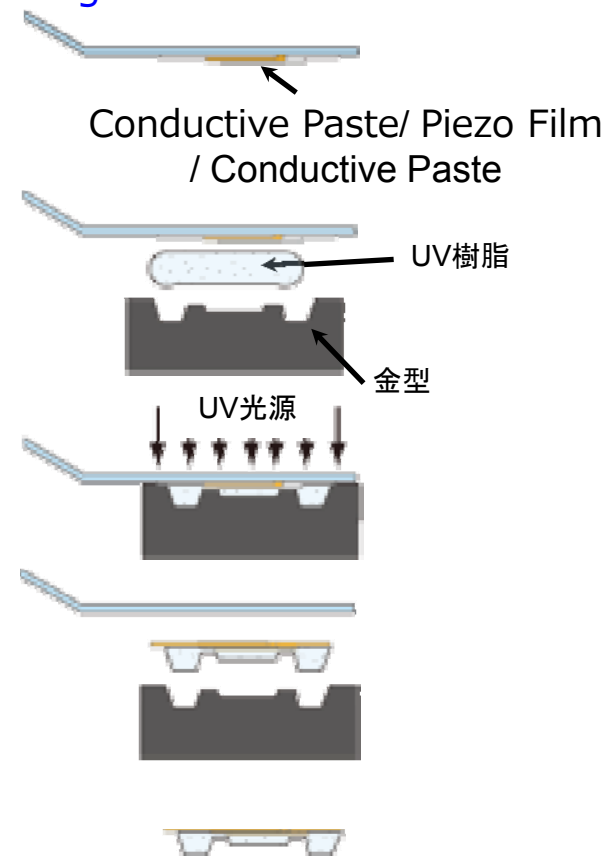
3) UV Cure



4) De-mold

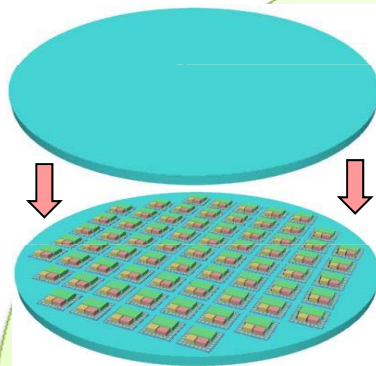


5) Device



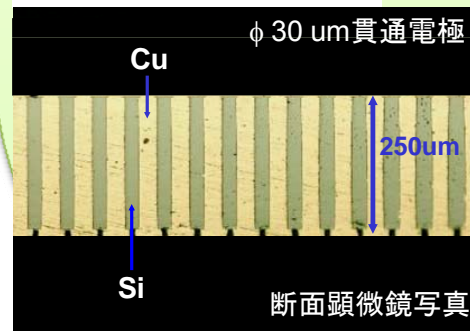
# High efficiency integrated MEMS production

## Large Area Wafer Level Package

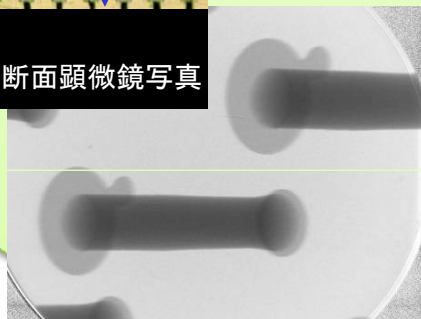


Low Temperature  
Large Area  
High Throughput

## 12" TSV Wafer



Deep Etching  
Electroplating



## Injection Molding

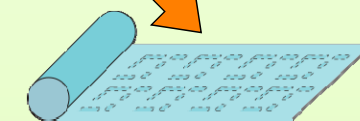
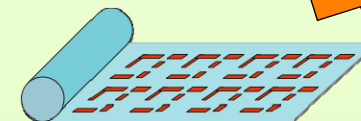
Mold with membrane for MEMS

MEMS device



Injection  
Molding

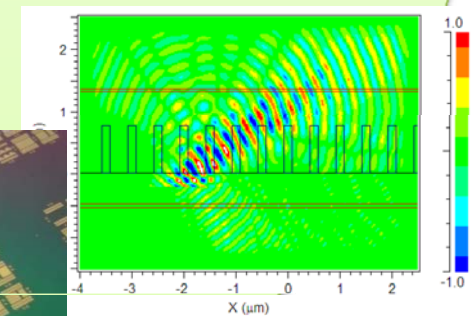
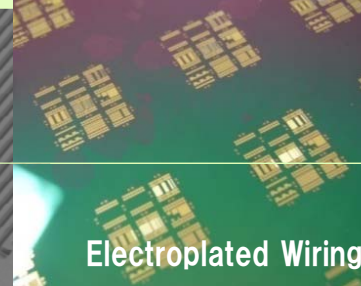
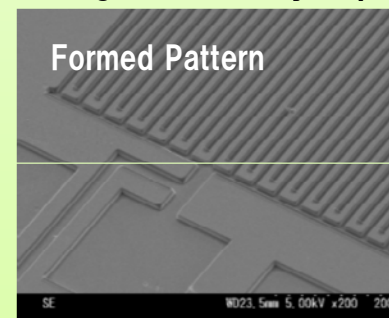
Printed wiring on film



## Nanoimprint Technology

Large Area, nm Pattern  
Low Cost, High Throughput

### Wiring Patterns by Imprint



New Function by  
nano-Structure

Low-cost, High-value, Low environmental Impact