

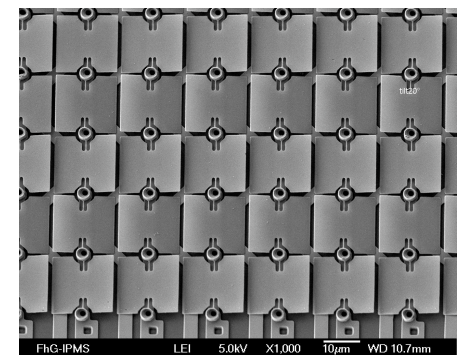
# Wafer-Level Heterogeneous Integration Techniques for MEMS and IC



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OF TECHNOLOGY

F. Niklaus, G. Stemme

**KTH - Royal Institute of Technology**  
**Microsystem Technology Lab**  
**Stockholm, Sweden**



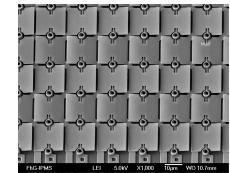
# KTH - Microsystem Technology Lab

**Head: Prof. Göran Stemme**



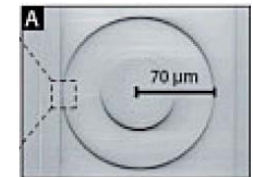
- **Micro- and Nanosystem Integration**

Assoc. Prof. Frank Niklaus



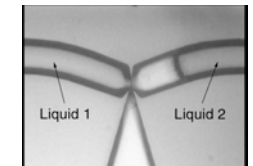
- **MicroOptic Sensors**

Ass. Prof. Hans Sohlström and Dr. Kristinn Gylfason



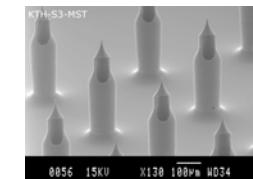
- **Micro-nano-biofluidic systems**

Prof. Wouter van der Wijngaart



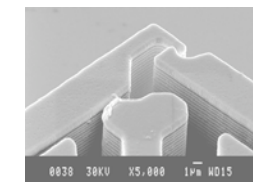
- **Medical MEMS**

Ass. Prof. Niclas Roxhed



- **RF-MEMS**

Assoc. Prof. Joachim Oberhammer



# Outline



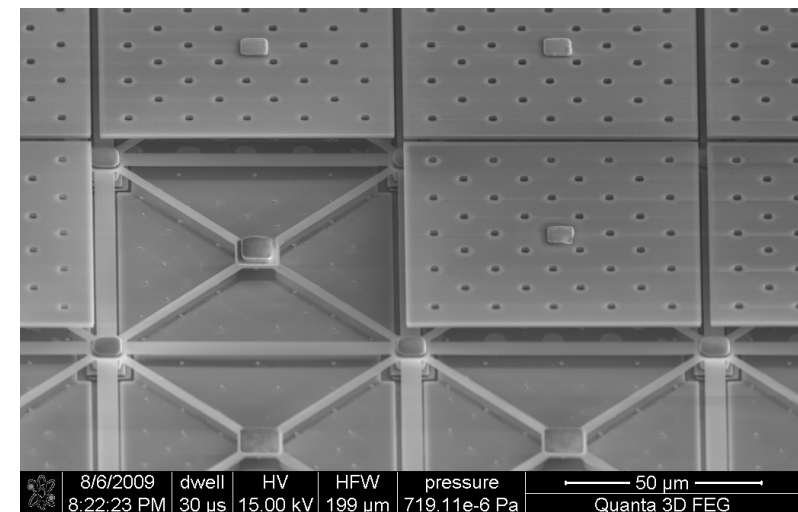
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- Heterogeneous MEMS Integration (SOIC)
- Device Applications
- TSV Technologies and Wafer-Level Packaging

# Heterogeneous Integration of MEMS and ICs

## Motivation / Advantages:

- New MEMS designs, functionalities and material combinations.
- High performance MEMS materials on standard foundry ICs.
- Very high integration densities for smaller and cheaper components.

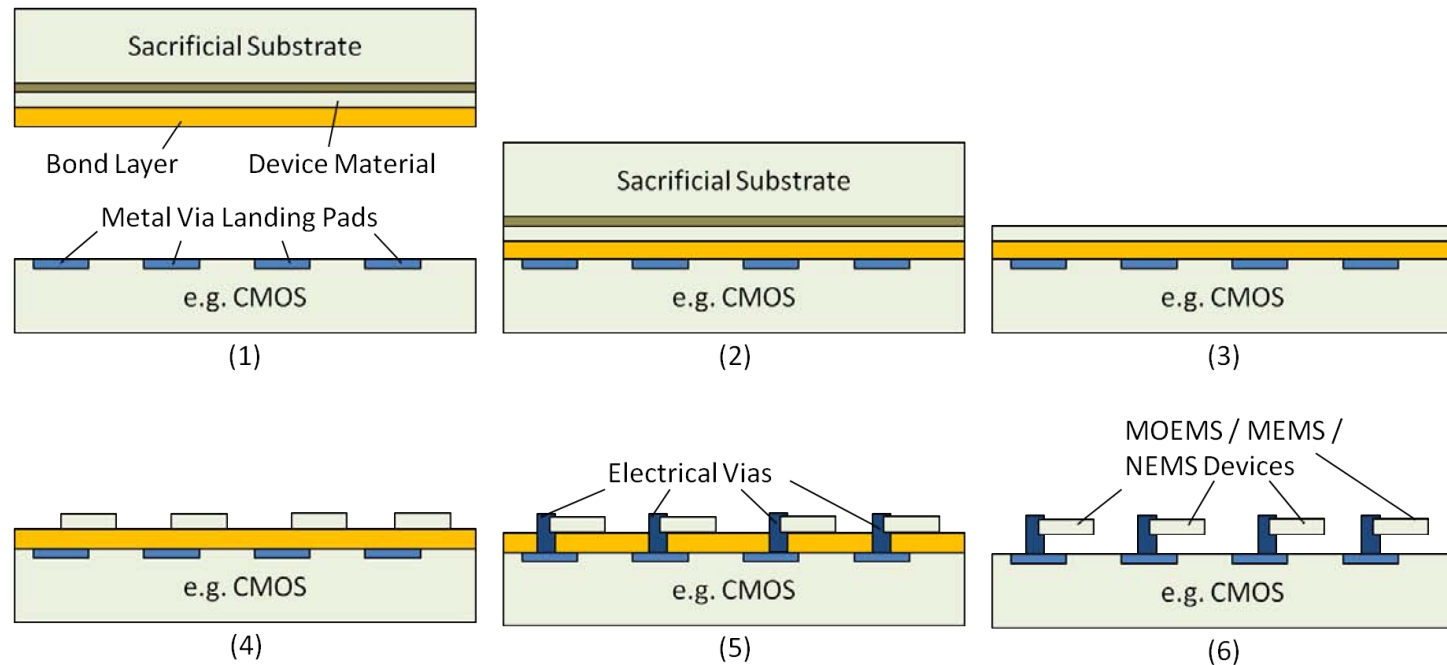


## Disadvantages:

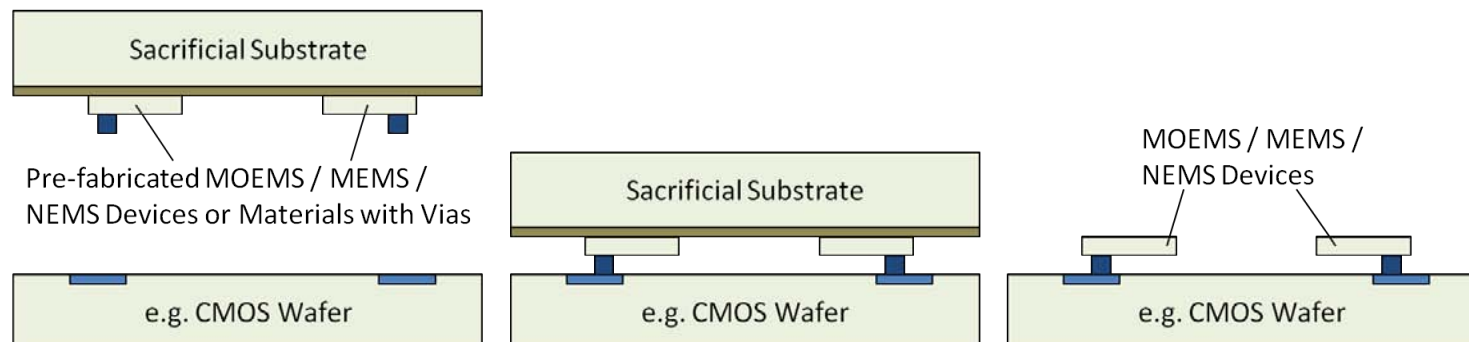
- May not be economic if IC and MEMS parts are very different in size.
- Penalty in yield accumulation when stacking several layers.

# Two Conceptual Approaches for Heterogeneous Integration of MEMS

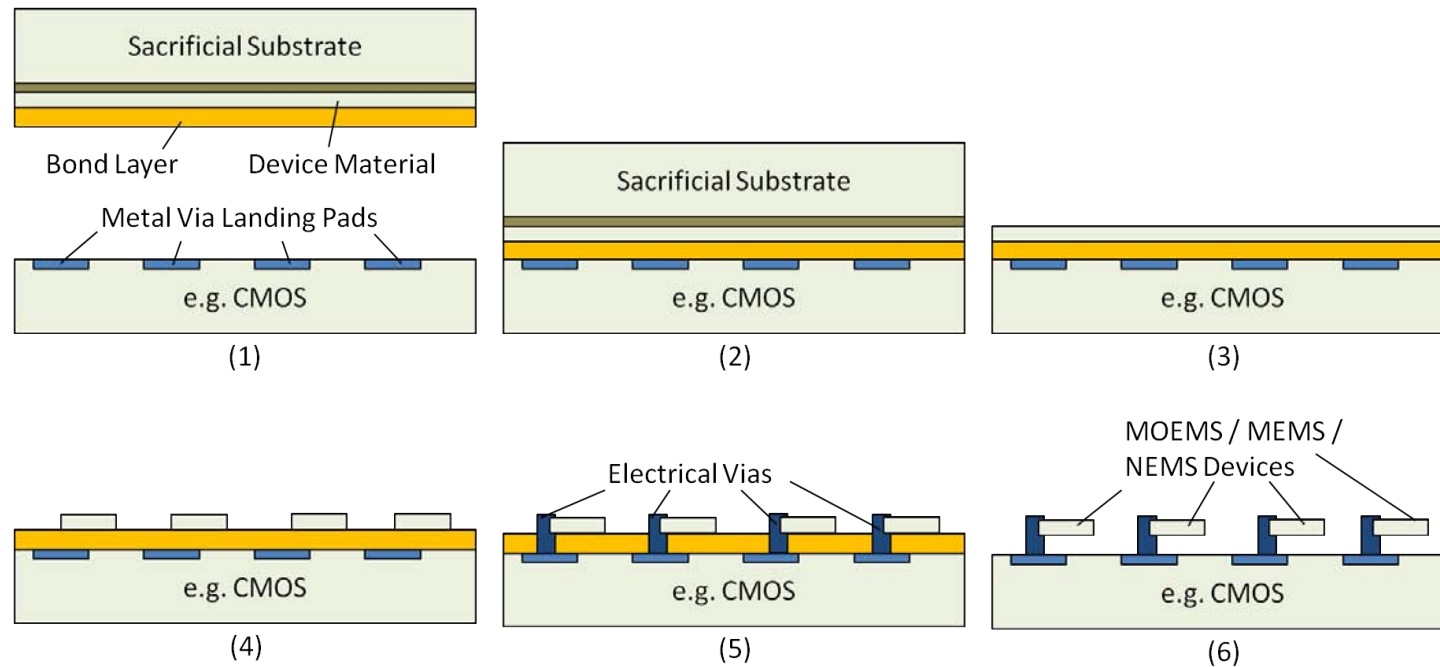
## Via Last Approach:



## Via First Approach:



# Silicon-On-Integrated-Circuit (SOIC) Platform



## Advantages:

- No wafer-to-wafer alignment.
- Extreme reduction of via and dimensions (sub  $\mu\text{m}$ ) possible.

## Disadvantages:

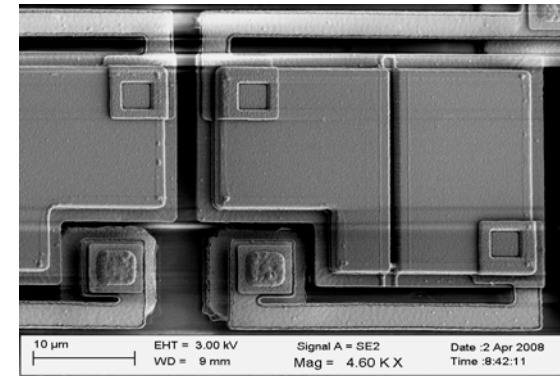
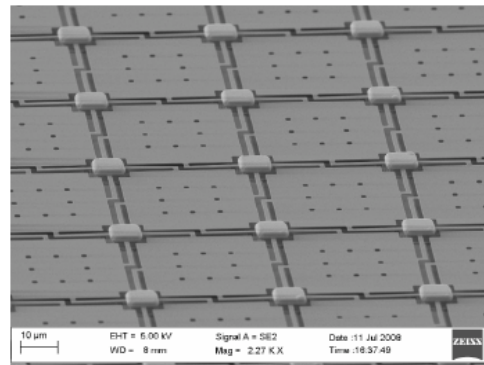
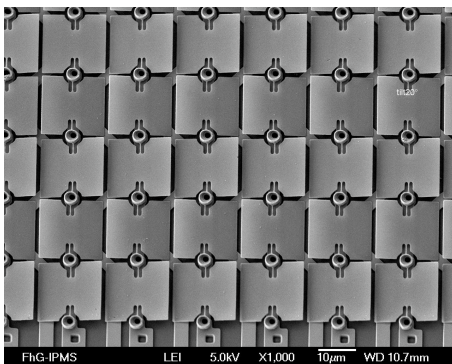
- MEMS devices must be processed after bonding.

# Via-Last SOIC Platform for MEMS Devices



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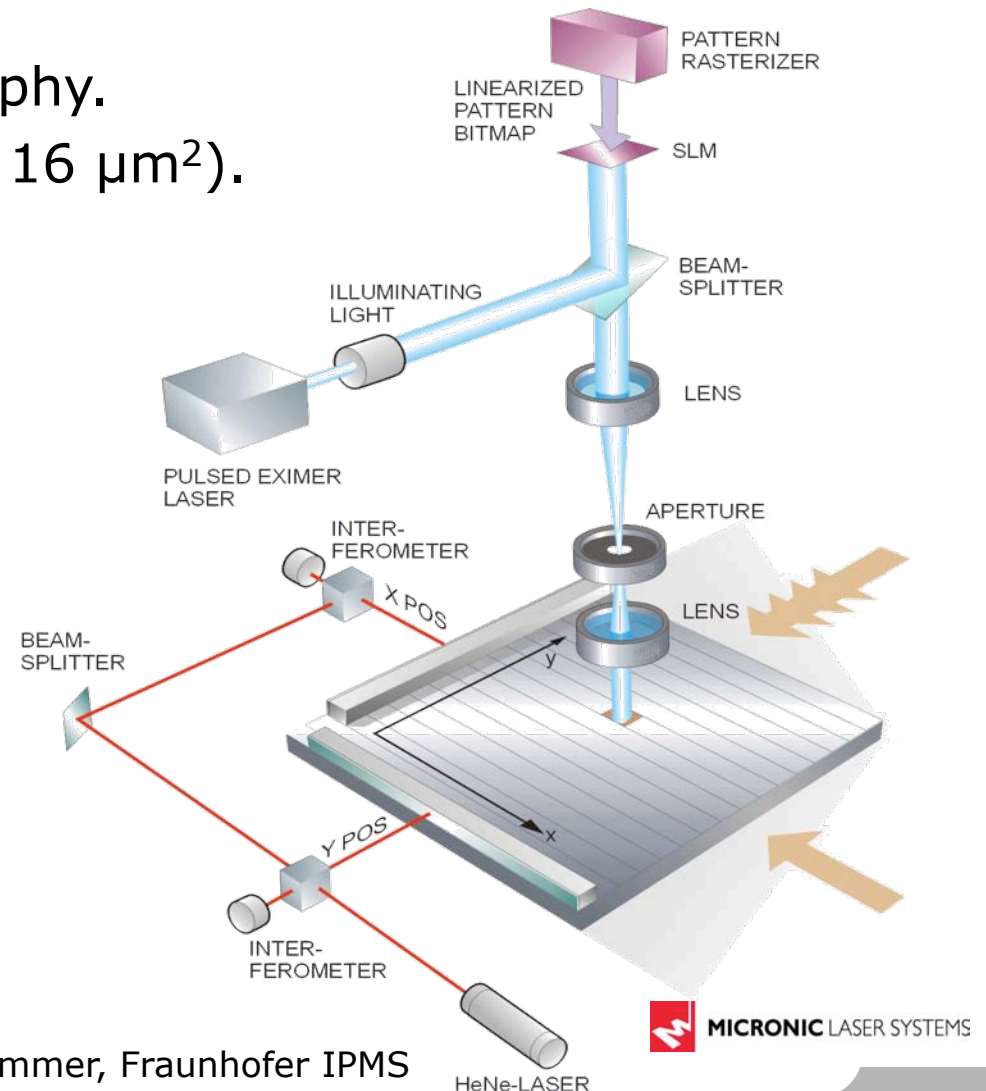
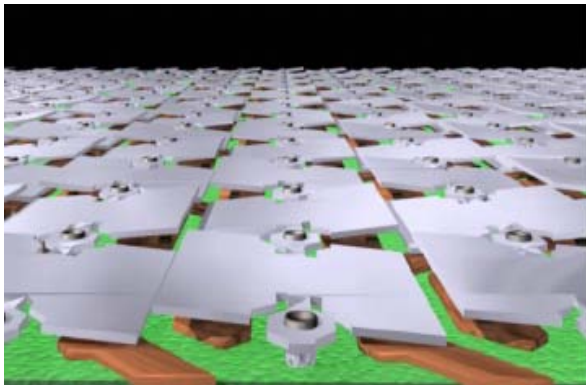
- Micro-mirror Arrays
- IR Bolometer Arrays
- RF MEMS devices





# Tilting Micro-Mirror Arrays (SLMs) for Maskless DUV lithography

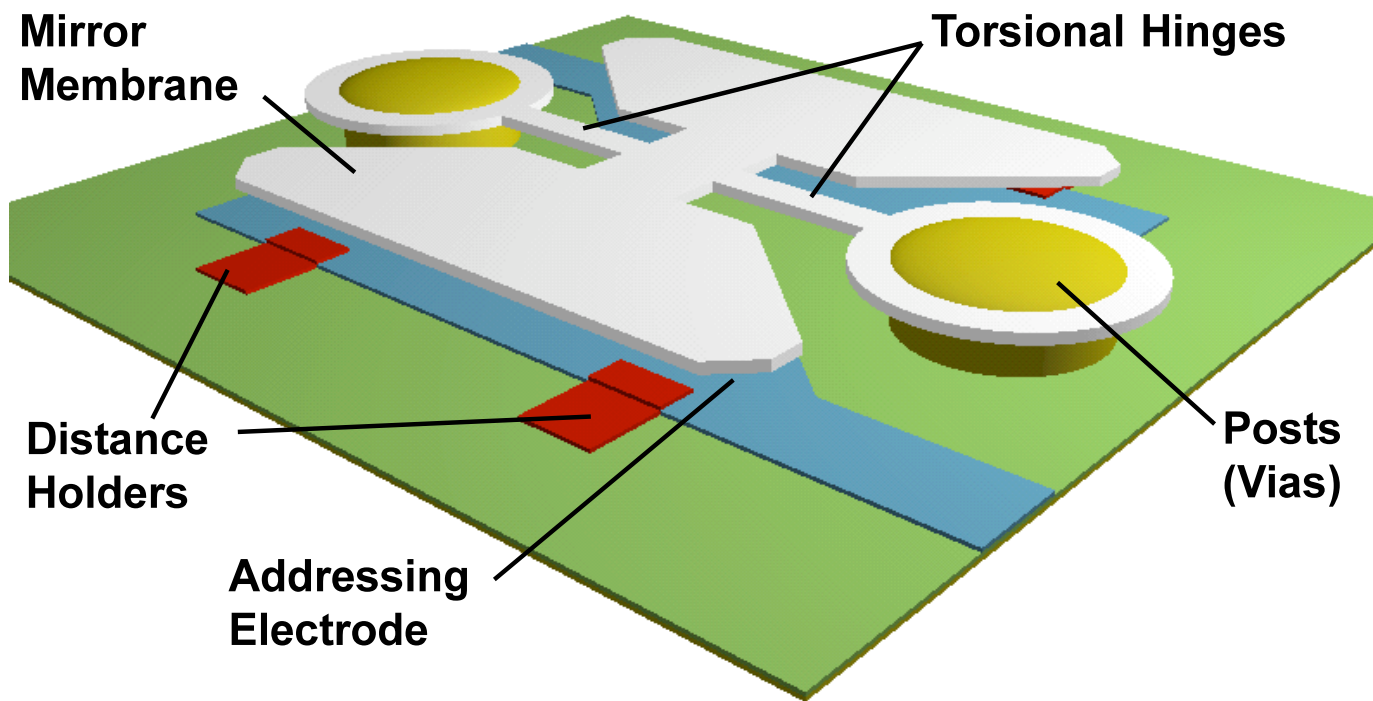
- Step and repeat maskless lithography.
- 1 million mirrors (mirror size  $16 \times 16 \mu\text{m}^2$ ).
- Single mirror actuation with underlying CMOS.
- Analogue tilt actuation in 16 steps (gray-tones) possible.



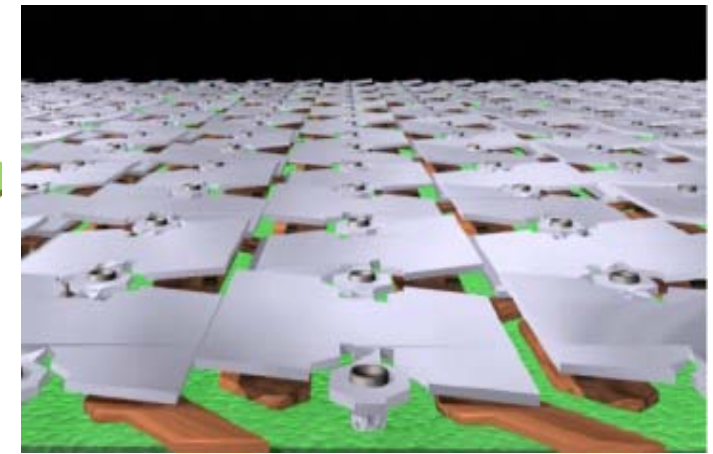
Source: Zimmer, Fraunhofer IPMS



# Torsional Micro-Mirror Array

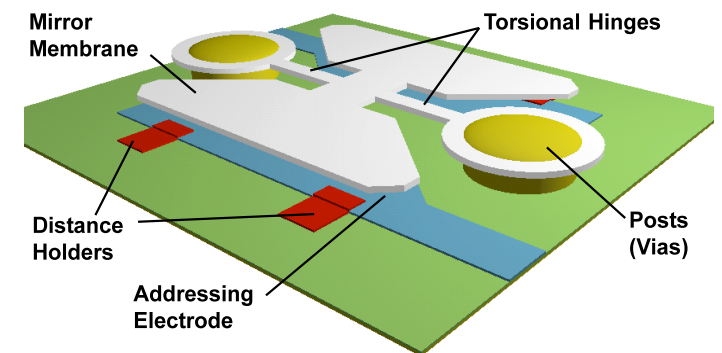
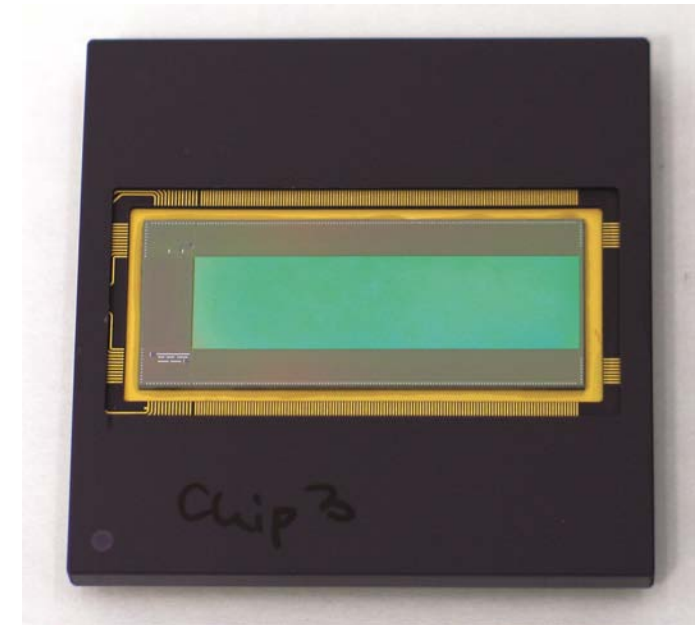
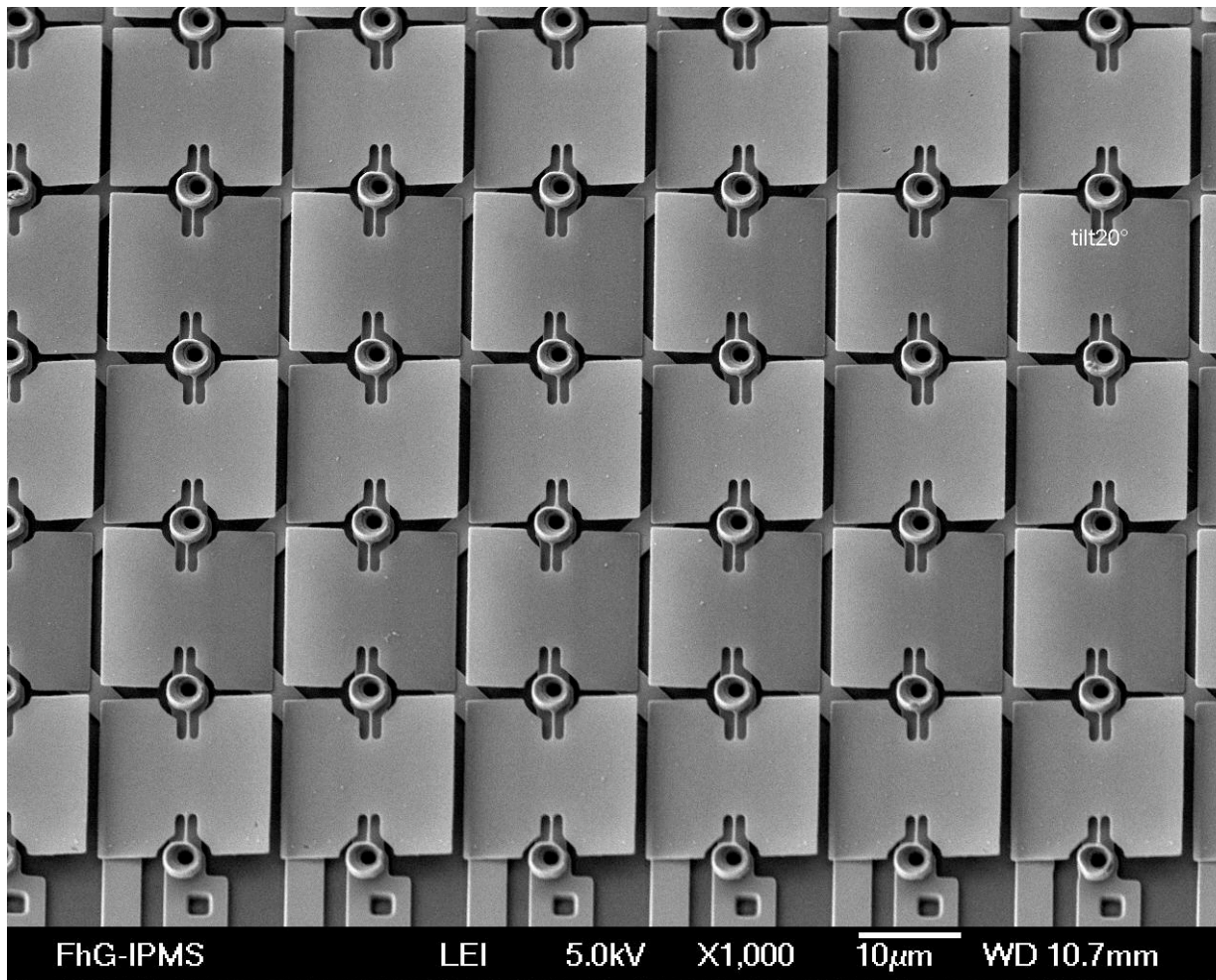


Source: Haasl, 2002



Source: Zimmer, Fraunhofer IPMS

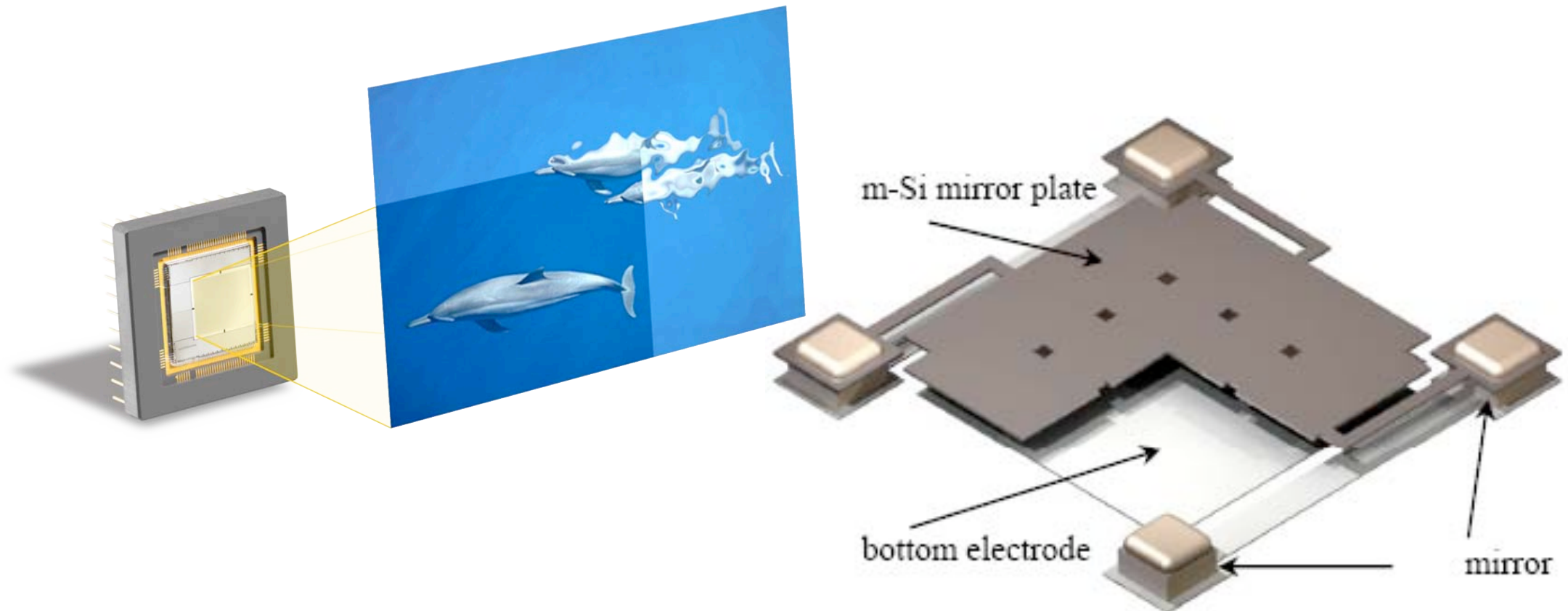
# 1 M-pixel Mono-Si Mirror Array on CMOS



Zimmer, Lapisa to appear MEMS 2011

# SLMs for Adaptive Optics in Astronomy and Microscopy

Wave-front correction using piston-type mirror arrays

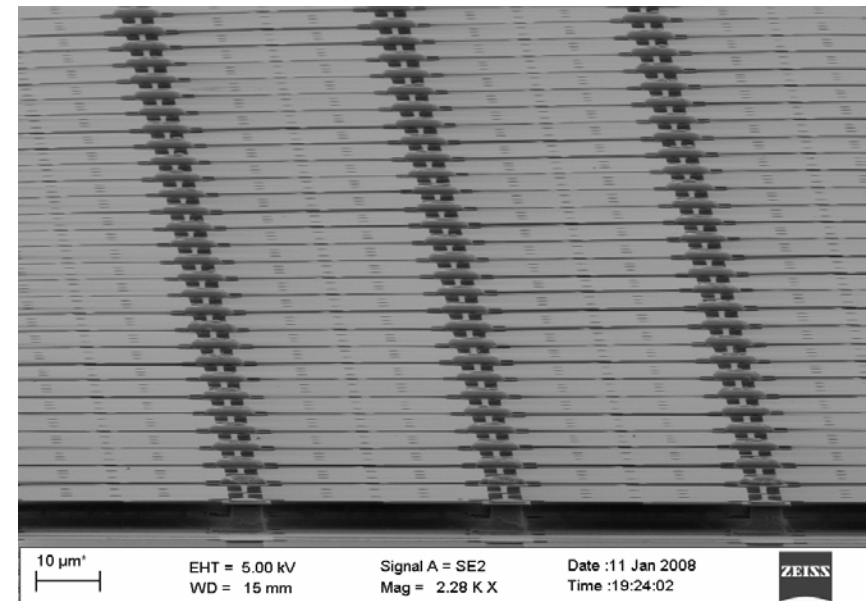
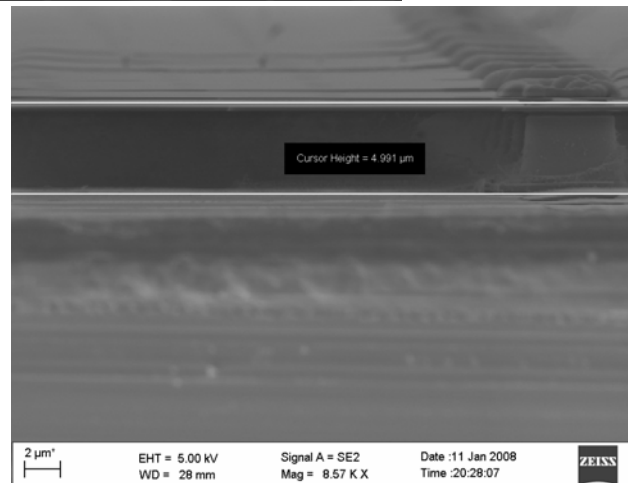
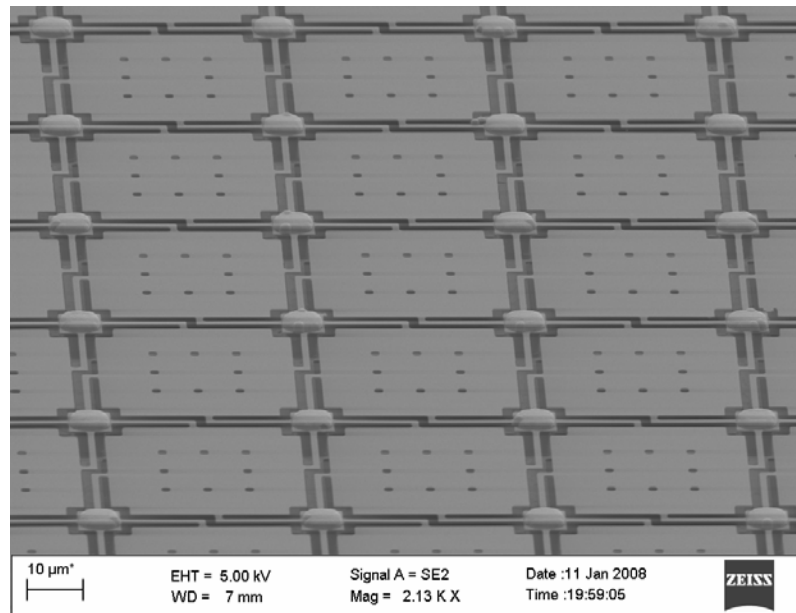


*Figure 1: Sketch of single mirror, mirror plate sectioned*

Source: Lapisa, KTH and Zimmer, Fraunhofer IPMS



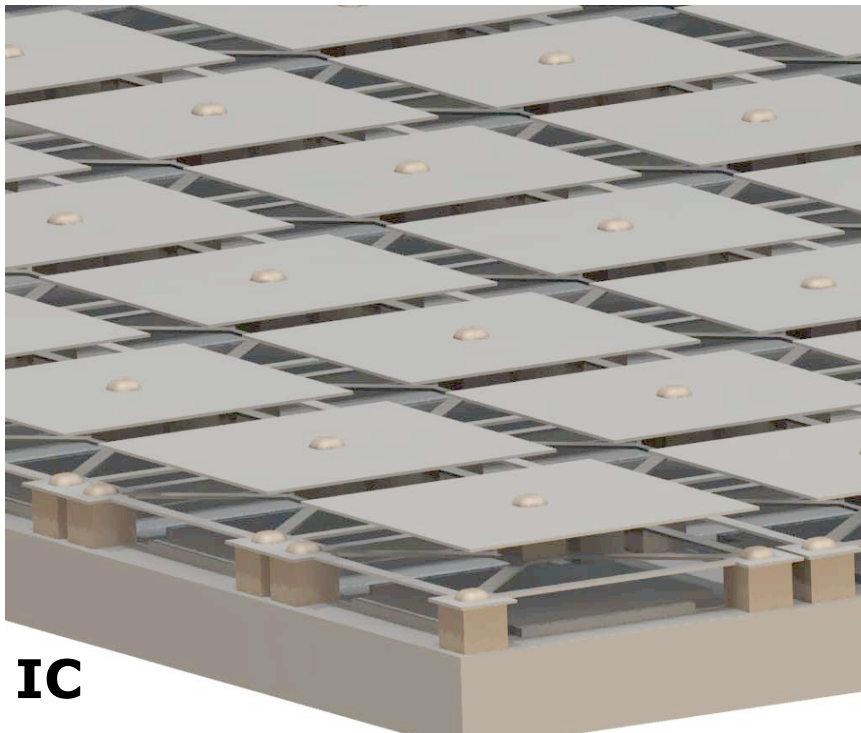
# Via-Last Heterogeneous Integration for Mono-Si Piston-Type Mirror Arrays



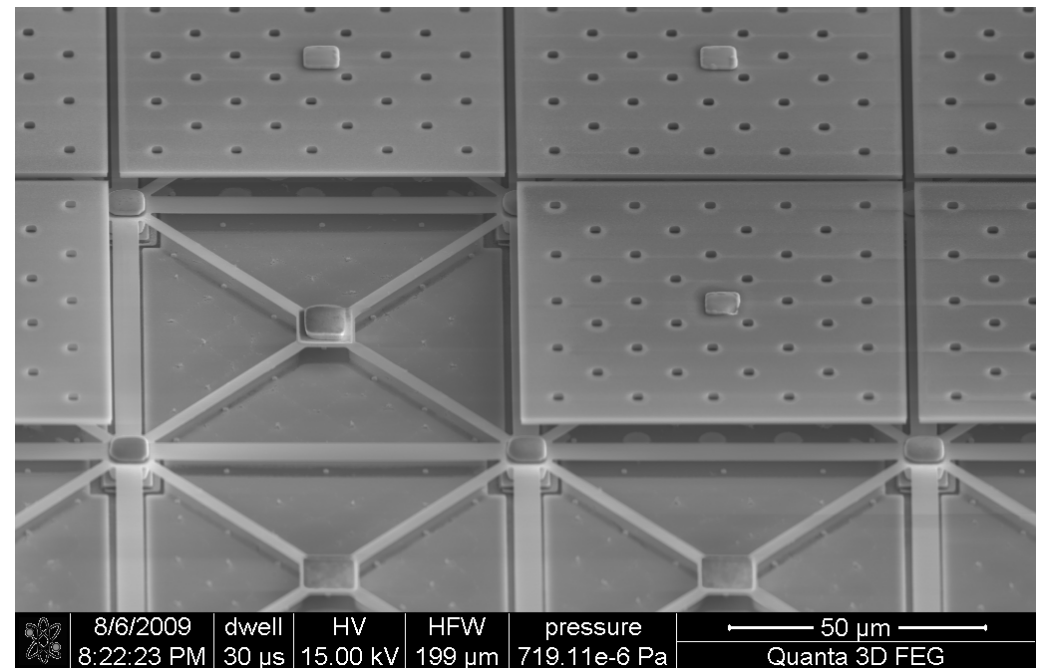
Lapisa KTH-MST, Gehner, Fraunhofer, 2008

# Via-Last Heterogeneous Integration for Piston-Type Mirrors Using Two-Step Layer Transfer

## MEMS

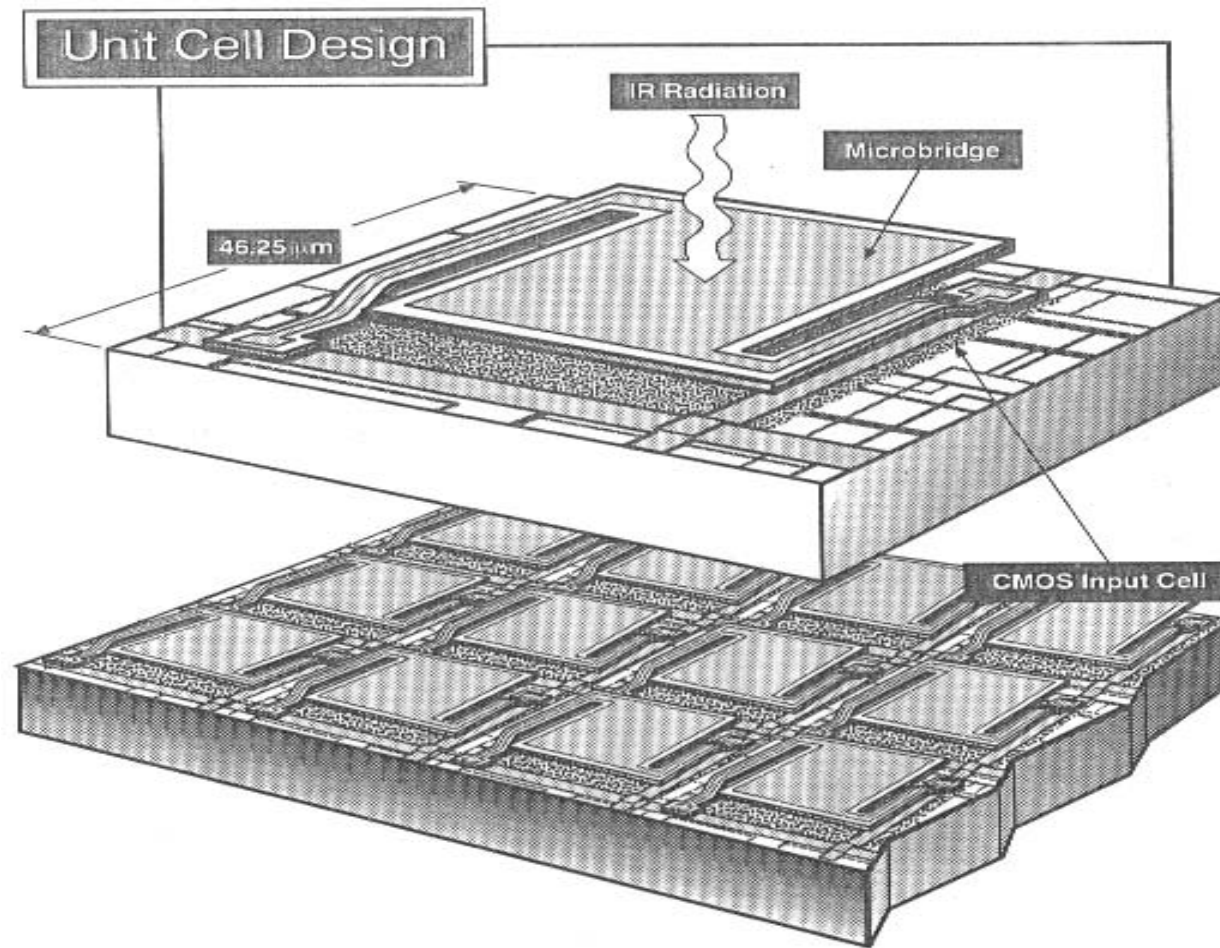


**CMOS IC**



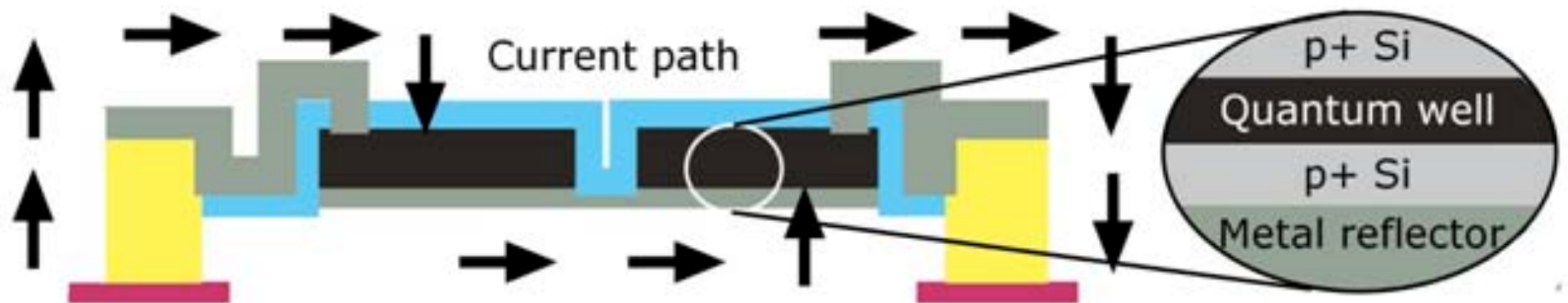
Lapisa KTH-MST, Gehner, Fraunhofer, to appear MEMS 2011

# Bolometer Array for IR Imaging



Buttler, 1995

# Design of QW Si/SiGe IR Bolometer

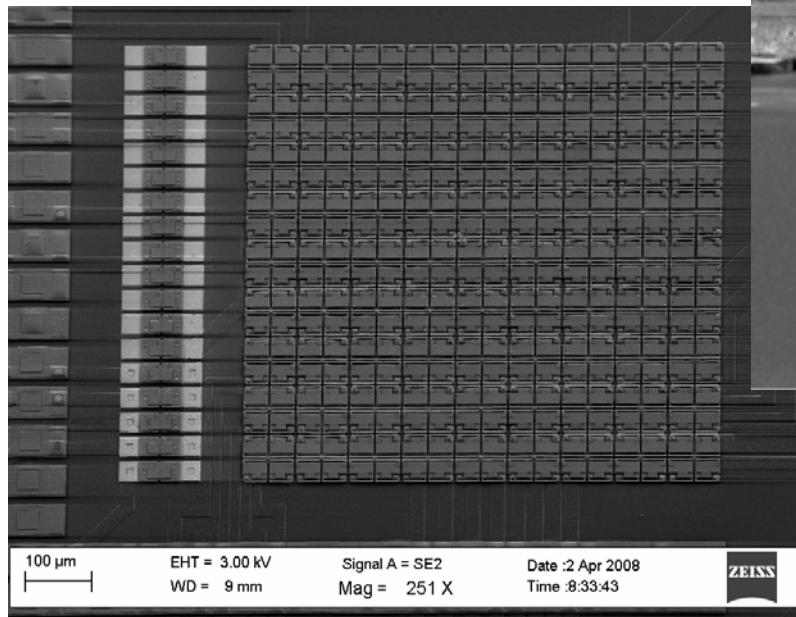


- Epitaxially grown QW Si/SiGe material with high TCR and low  $1/f$  noise.
- Direct deposition of crystalline Si/SiGe QW on CMOS is not possible.

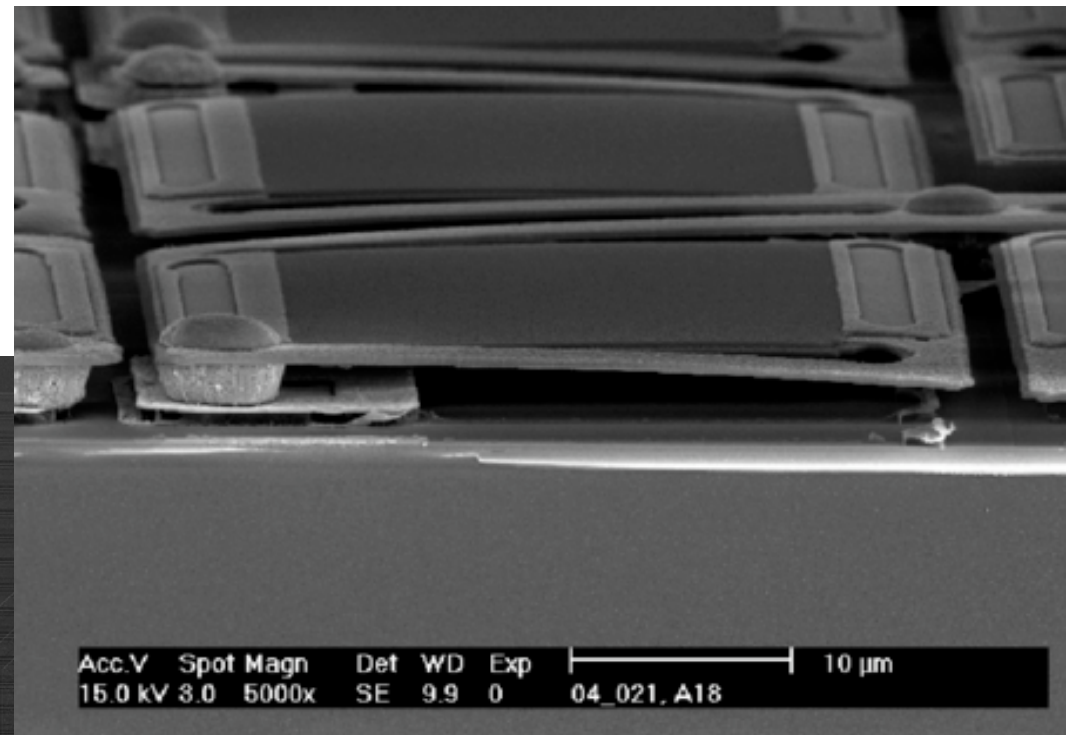
=> Via-last SOIC MEMS heterogeneous integration



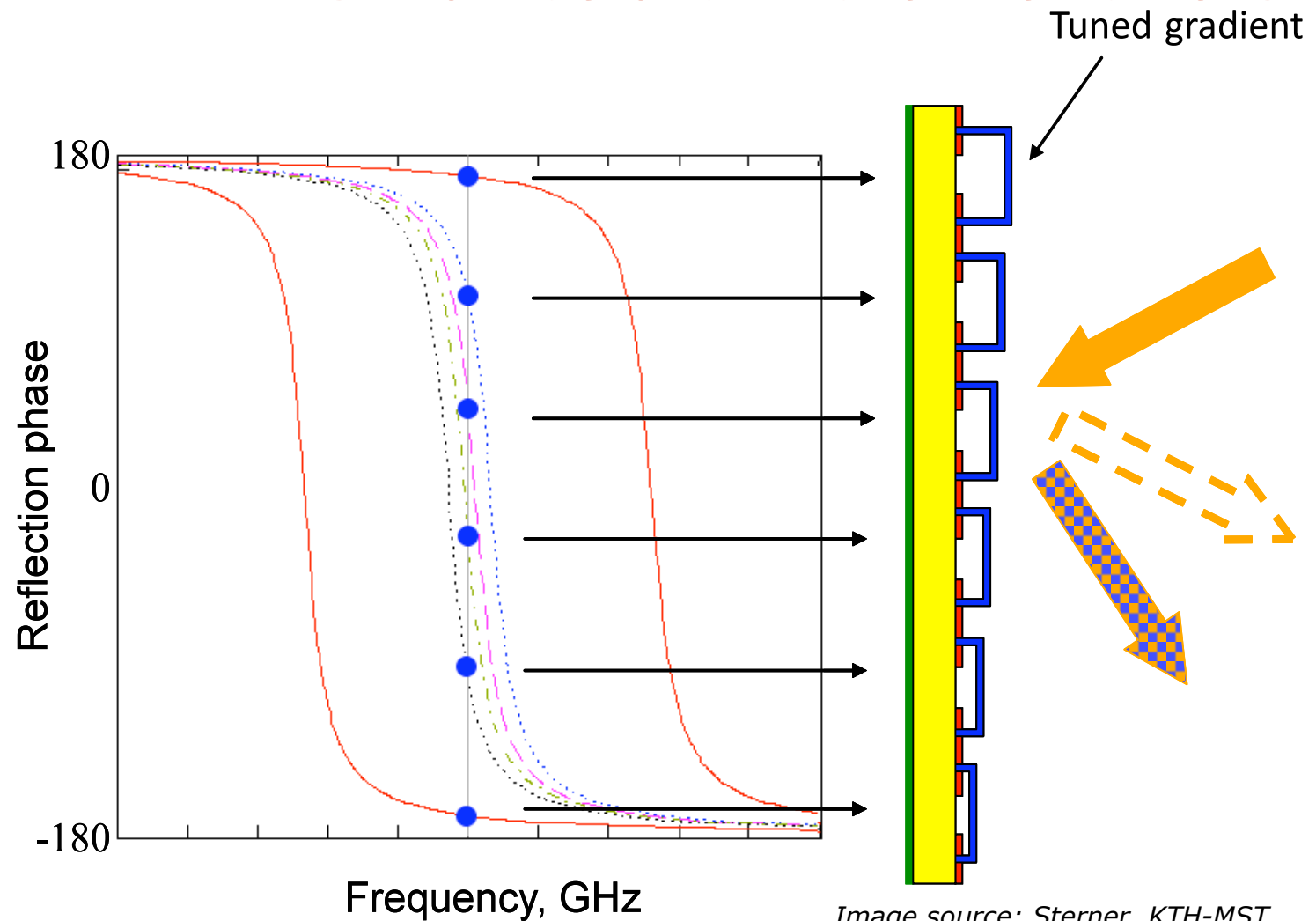
# Heterogeneously Integrated QW SiGe Bolometers on Fan-Out-Board



16x16 IR Bolometer Array



# RF MEMS: Radar Beam Steering with MEMS Tuneable Metamaterials



# RF Metamaterial Design

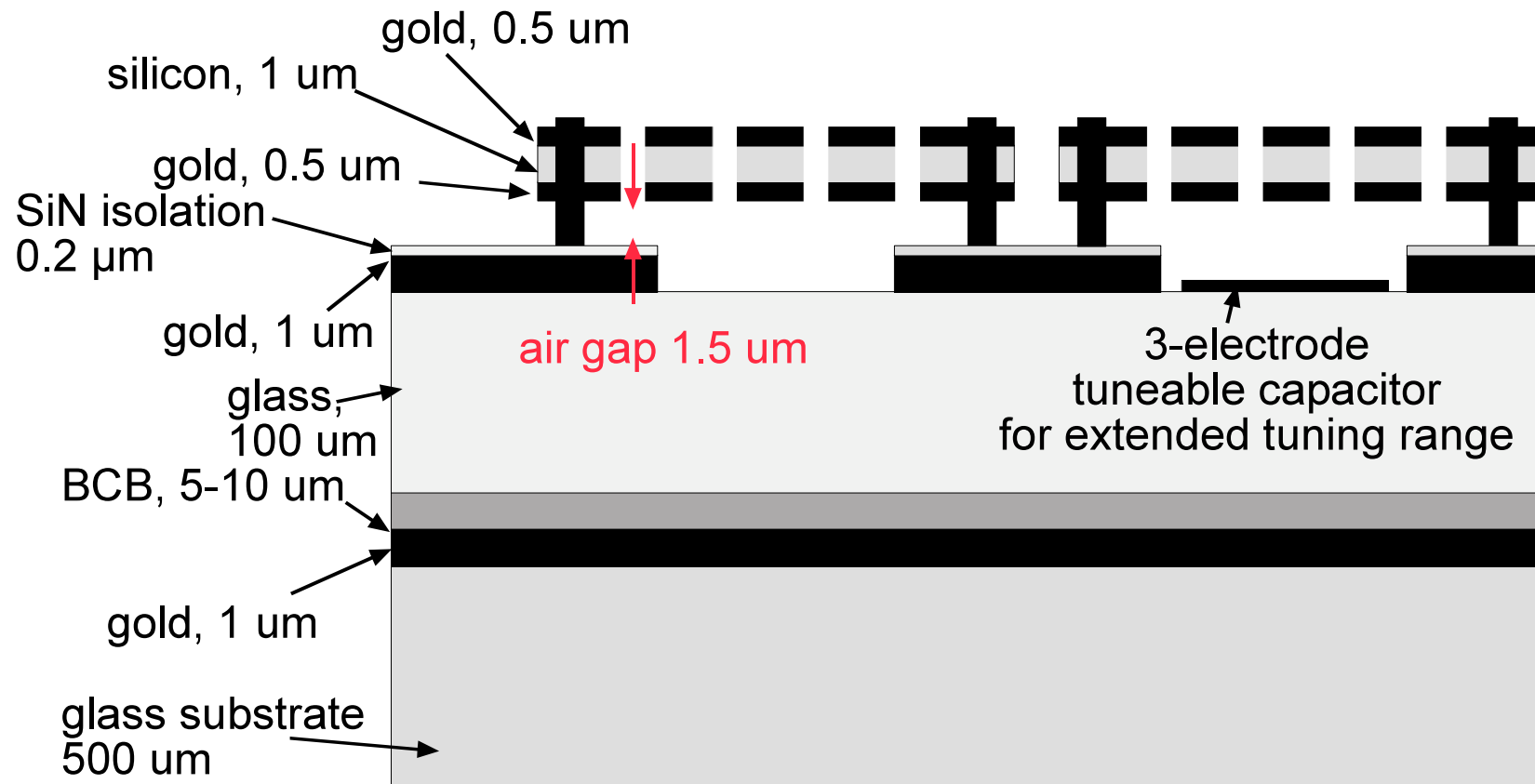
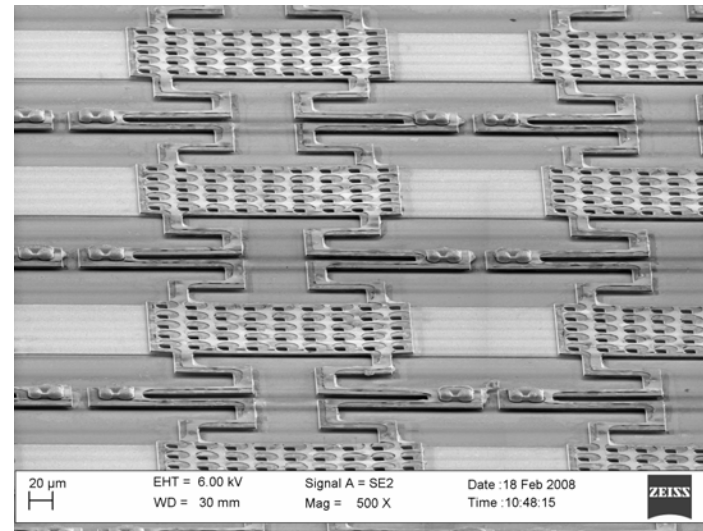
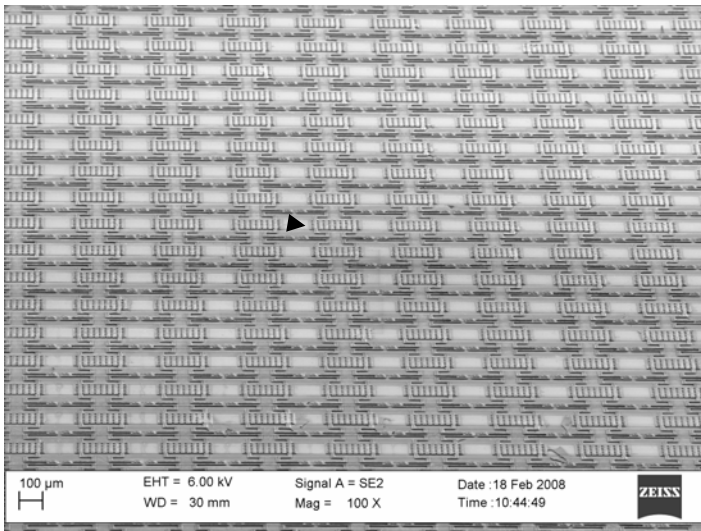


Image source: Sterner, KTH-MST

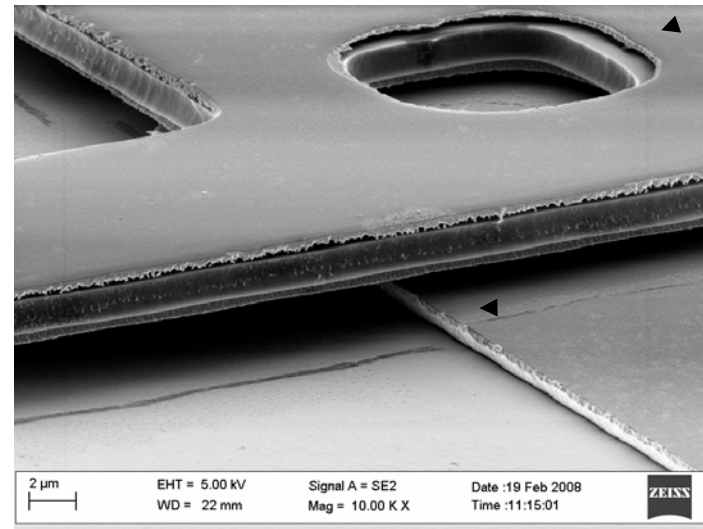
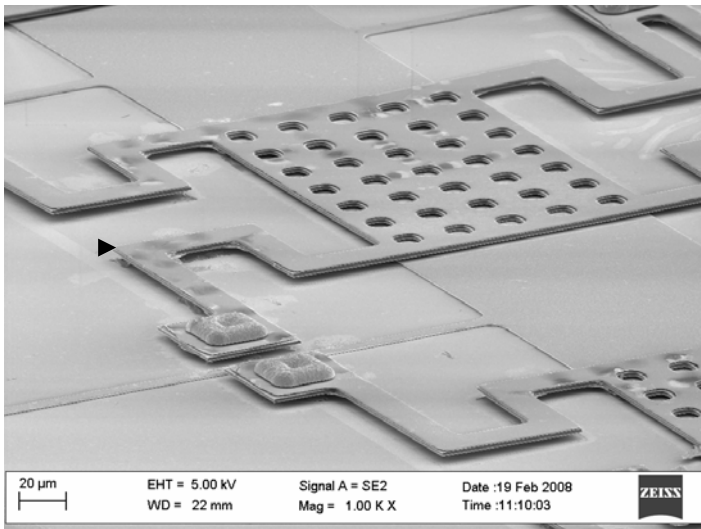
# RF Metamaterial Fabricated Device

Array of  
200×52  
elements



Etch hole

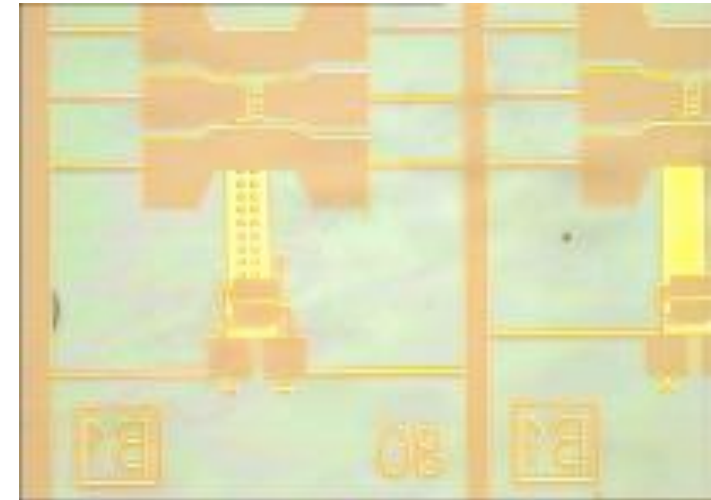
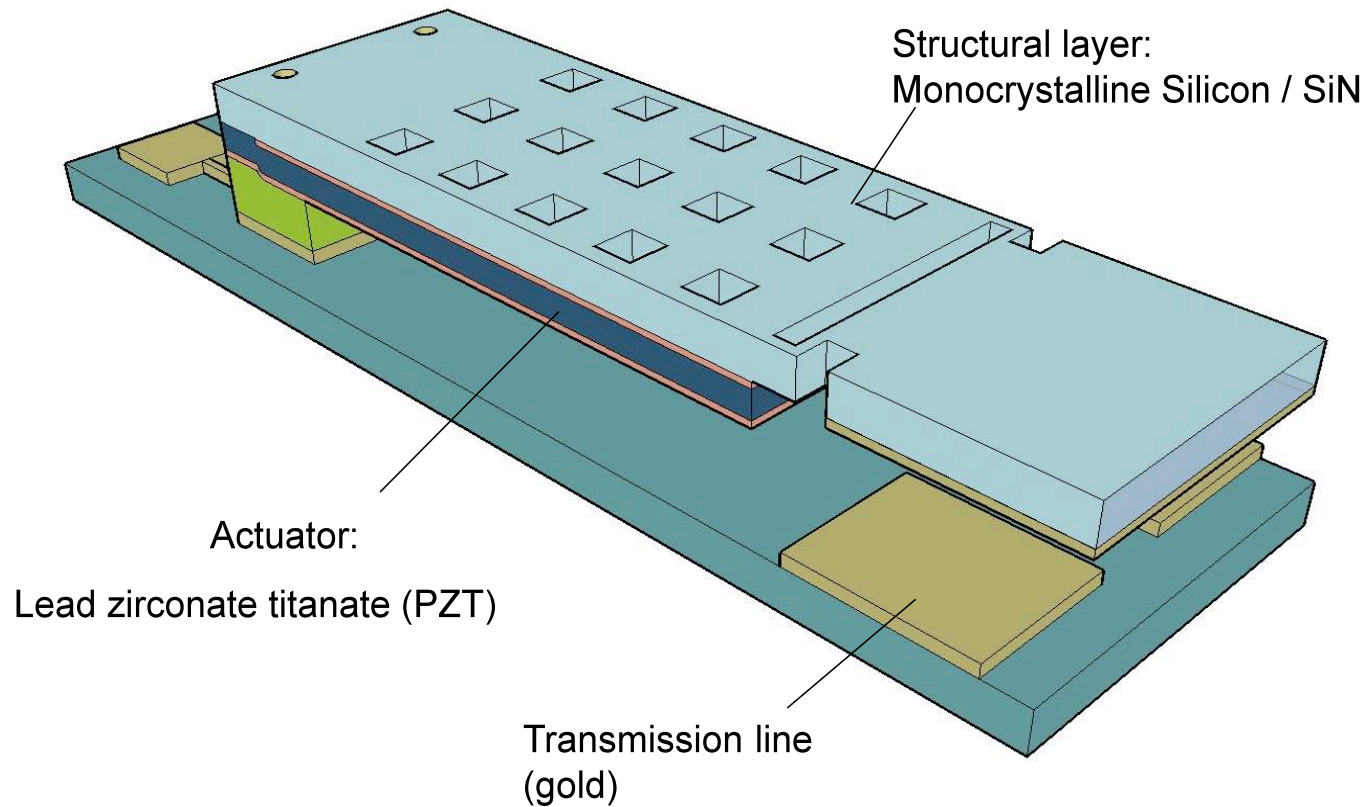
Springs



Gap of  
~1.5 μm

Image source: Sterner, KTH-MST

# PZT RF-MEMS Switch

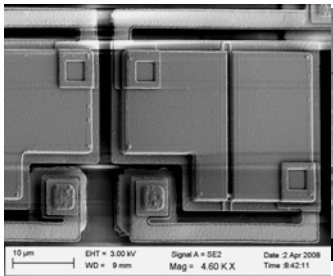


*Image source: Saharil, KTH*

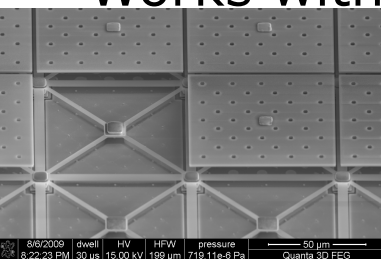


# Advantages of SOIC Integration Platform

- High performance MEMS materials can be integrated on any foundry ICs.
- No ASIC wafer surface planarization required.
- Small parasitic capacitances for e.g. capacitive MEMS.
- Dry etch of polymer for MEMS release.
- MEMS foundry compatible.
- No wafer-to-wafer bond alignment required.
- Low-cost and high yield process.
- Works with all wafer materials.



m-SiGe on CMOS



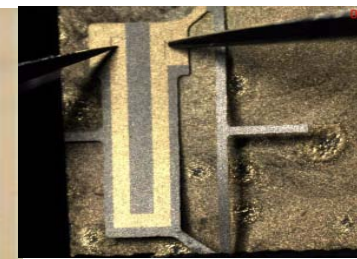
m-Si on CMOS



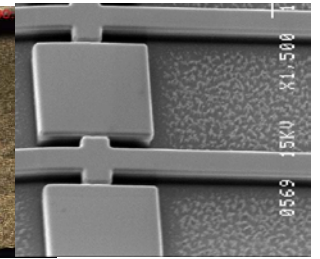
Glass on Si



PZT on Si

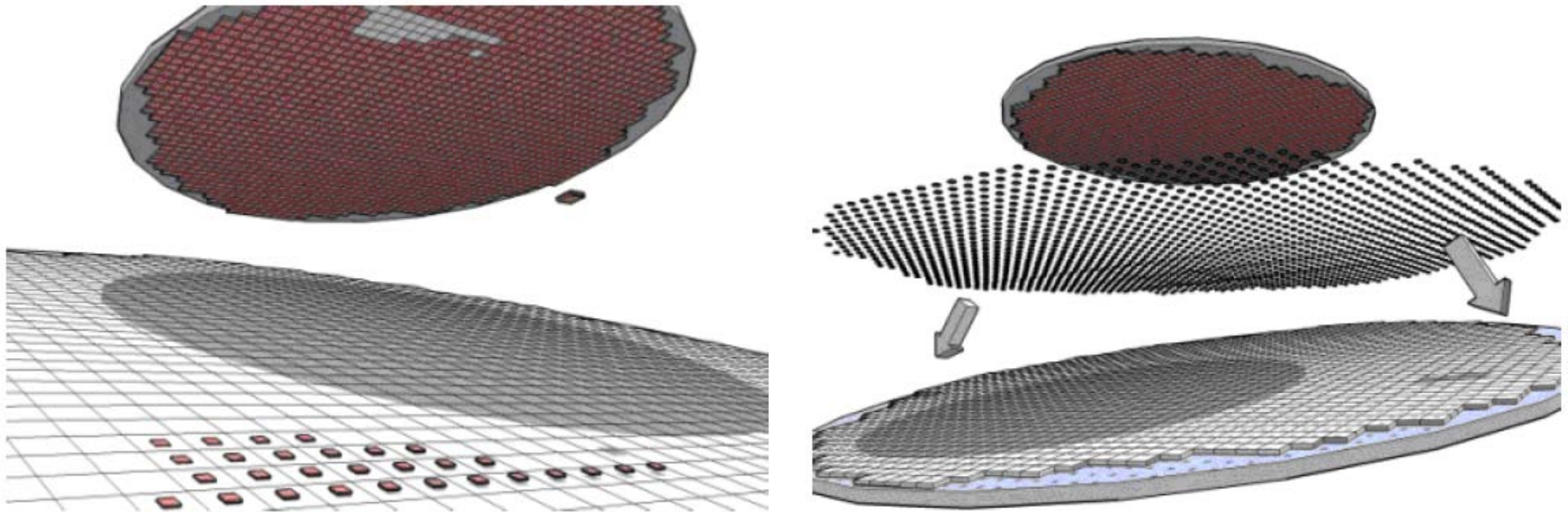


SMA on Si



GaAs on Si

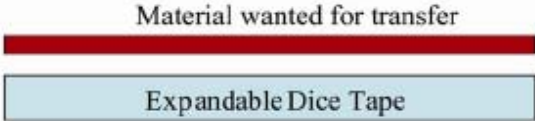


# Heterogeneous Integration of Different Wafer Sizes

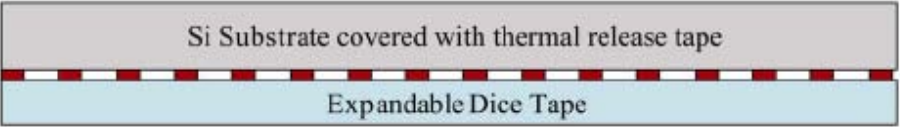
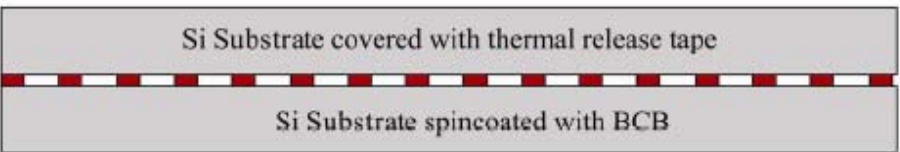
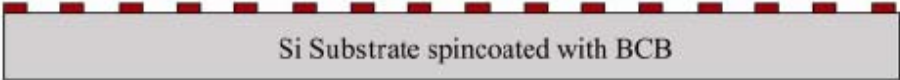


*Image source: Forsberg, Proc. MEMS 2011, KTH*



# Heterogeneous Integration Using Different Wafer Sizes

1.   
Place the material to be transferred on an expandable dice tape.
2.   
Dice the wafer into small chips.
3.   
Expand the tape to the wanted chip separation.

4.   
Transfer the diced chips to Si substrate covered with a fastened thermal release tape
5.   
Transfer the dies to a 200 mm silicon wafer using adhesive wafer bonding.
6.   
The dies are bonded to Si substrate using BCB. The thermal release tape loses its adhesion during bonding and is removed.

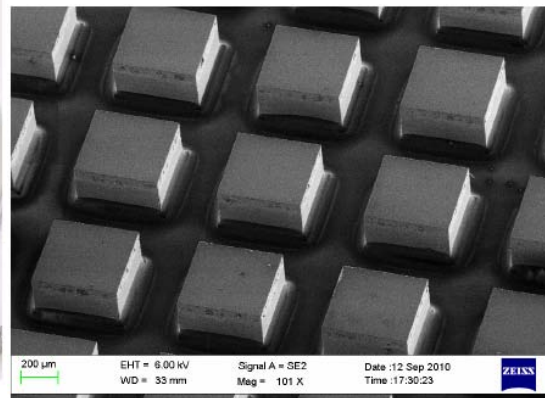
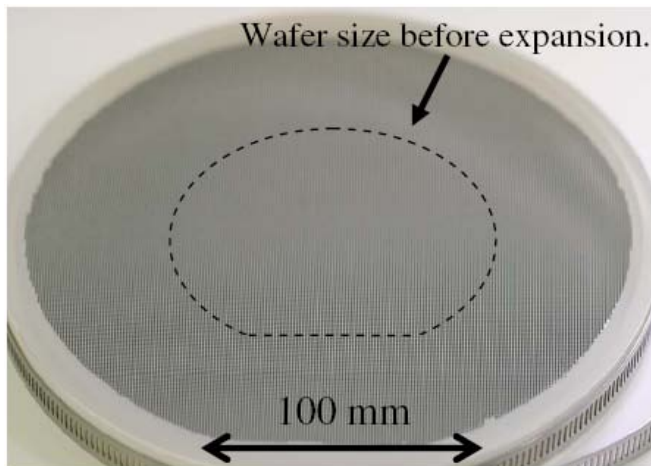


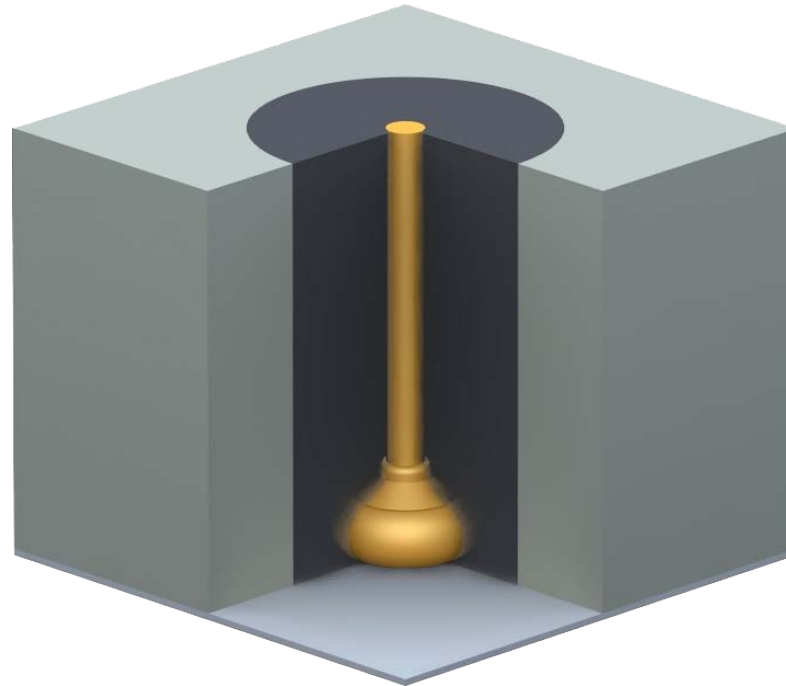
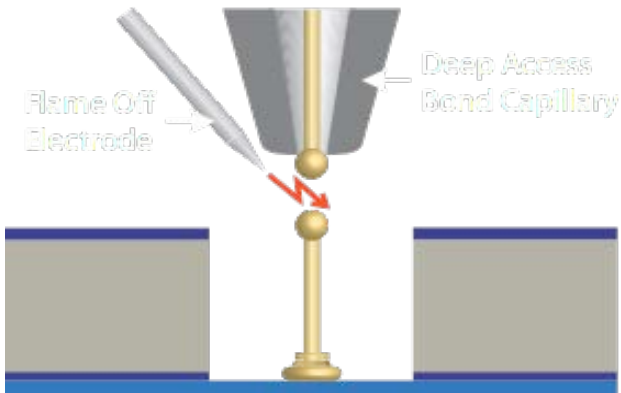
Image source: Forsberg, 2011, KTH

# Wire-Bonded Through-Silicon Via (TSV) Platform

1) Via hole formation



2) Wire bonding



3) Filling with dielectric



4) Grinding, polishing & metallization



Image source: Fischer, Proc MEMS 2010, KTH

# Wire-Bonded Through-Silicon Vias (TSVs)

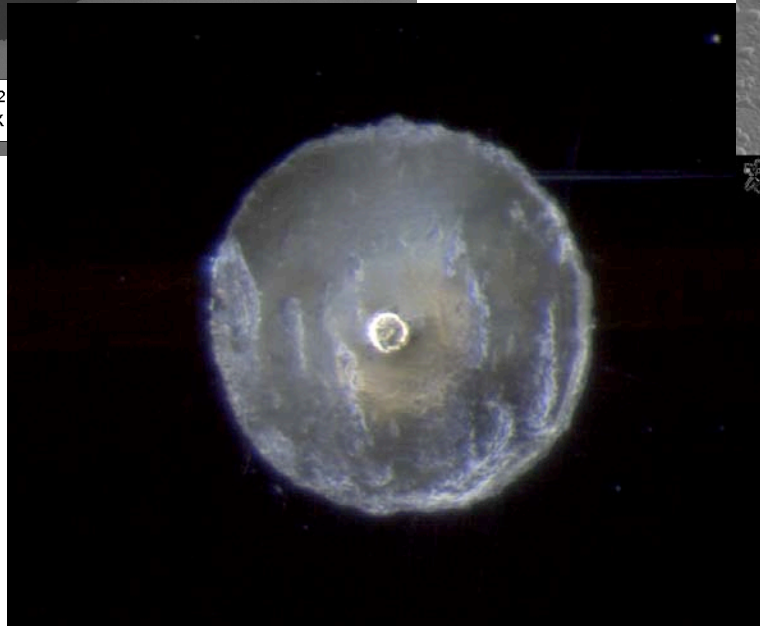
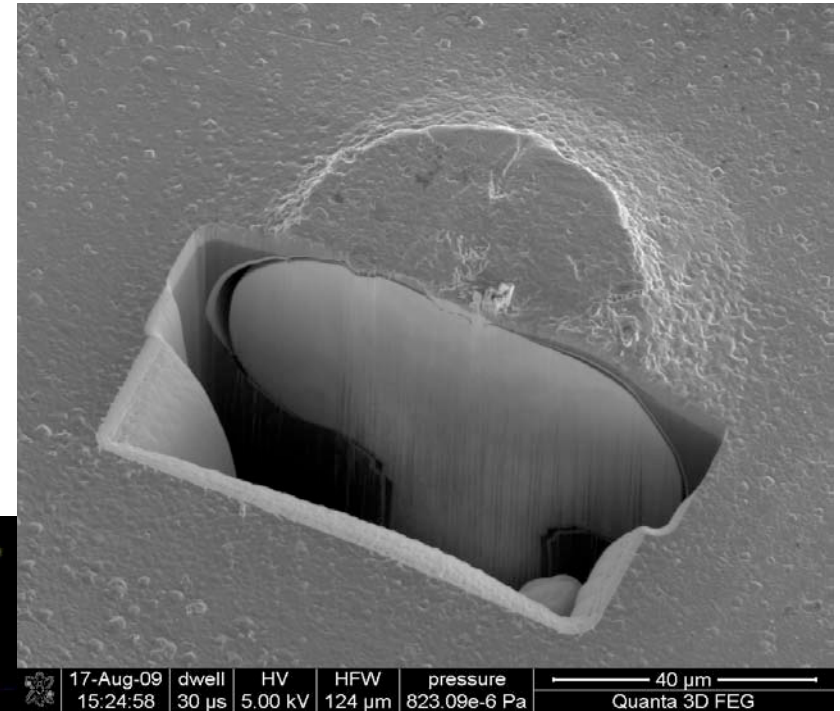
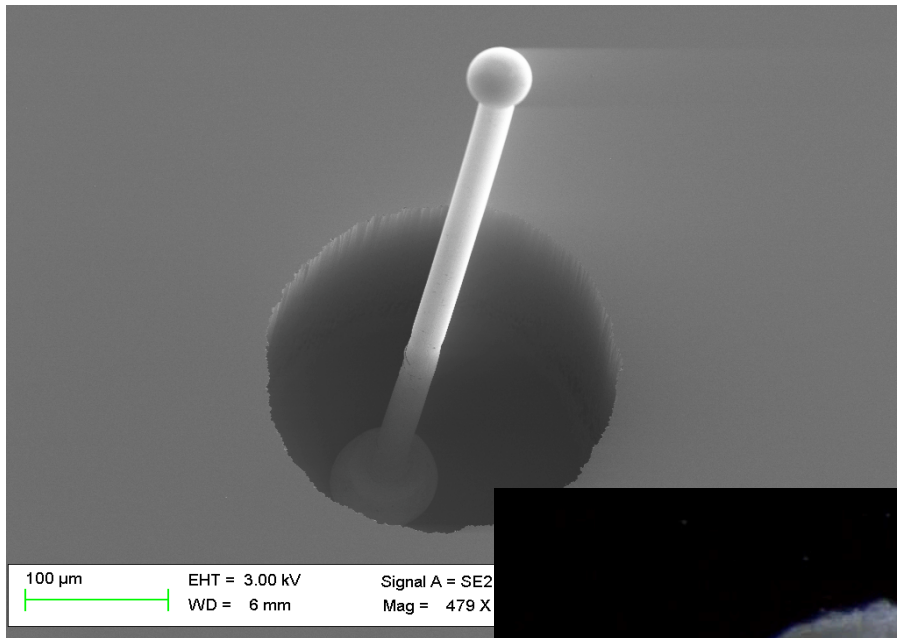


Image source: Fischer, Proc MEMS 2010, KTH

# Fabrication of High-Aspect Ratio TSVs by Magnetic Assembly of Metal Studs

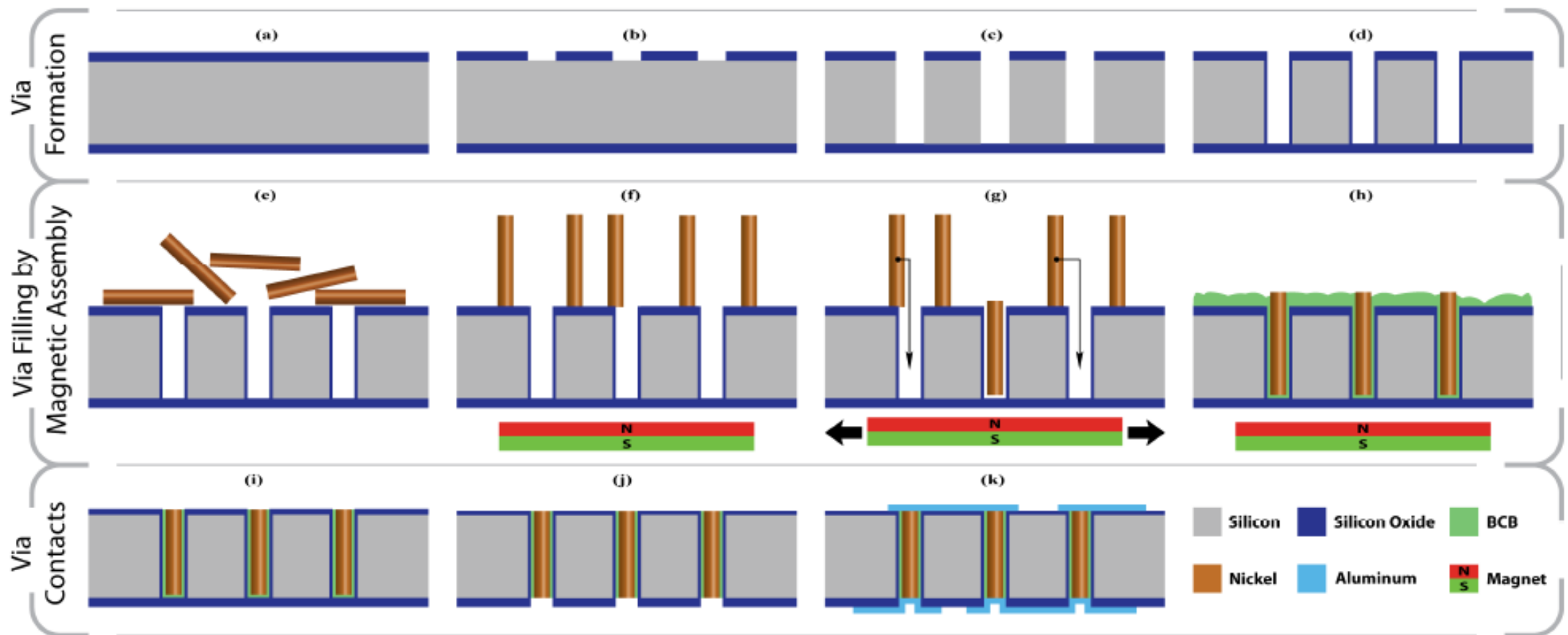


Image source: Fischer, Proc MEMS 2011, KTH

# High-Aspect Ratio nickel TSVs

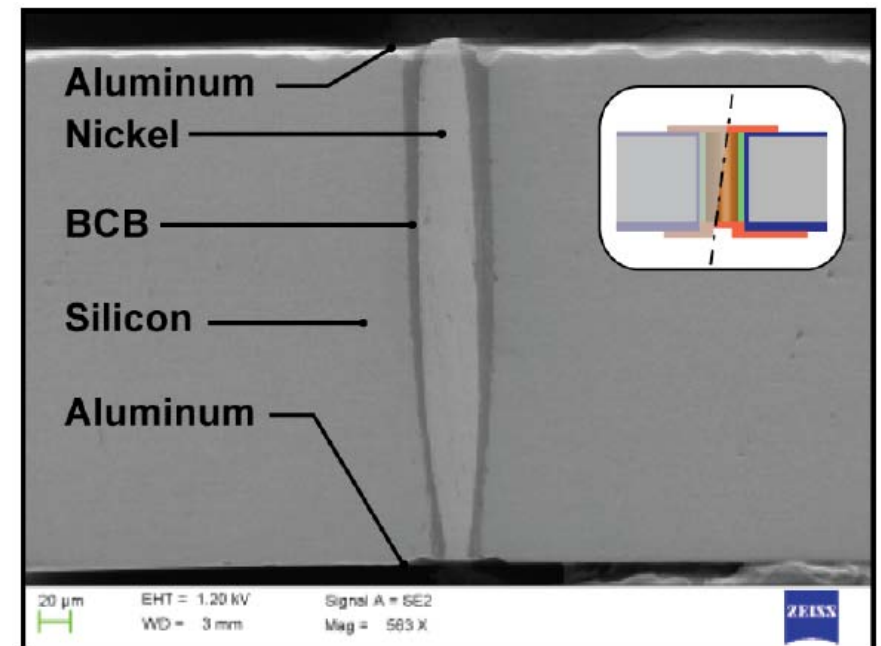
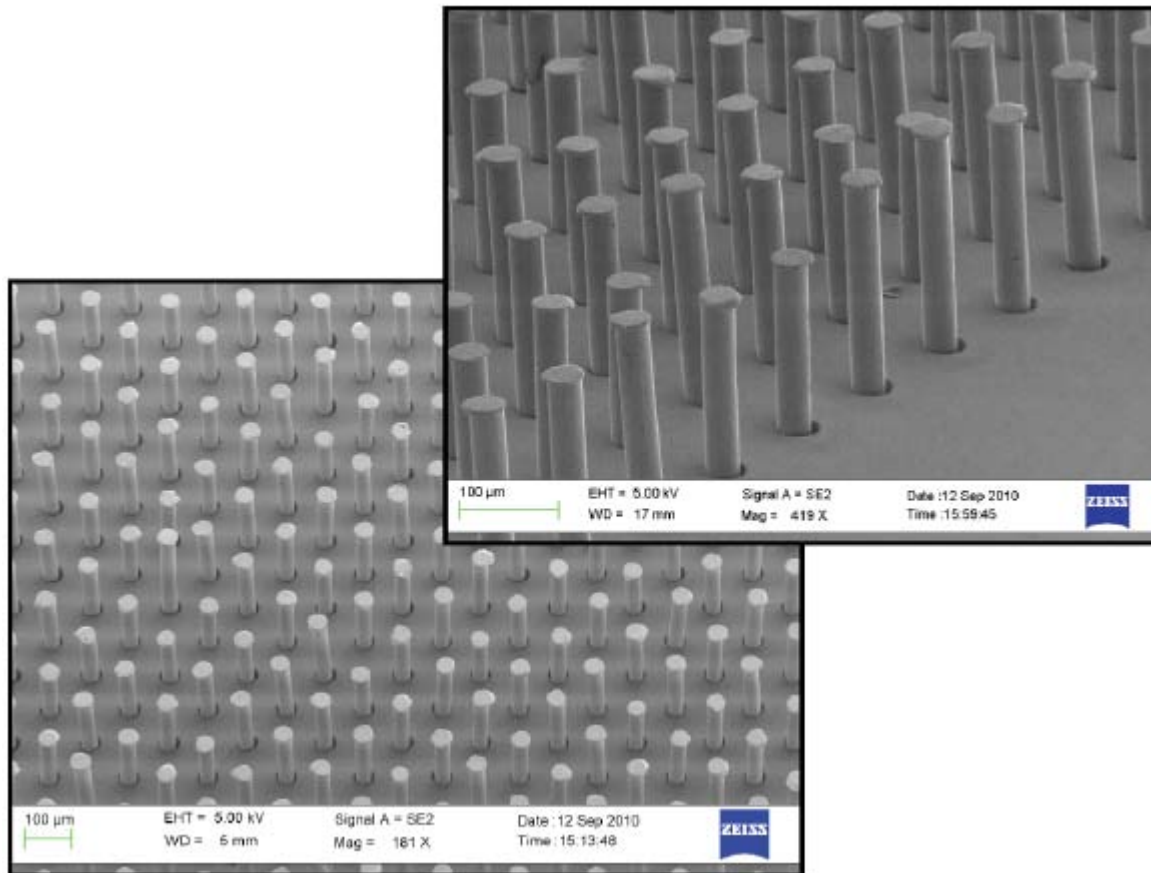


Image source: Fischer, Proc MEMS 2011, KTH

# Wafer-Level Vacuum Sealing by Cold Metal Welding

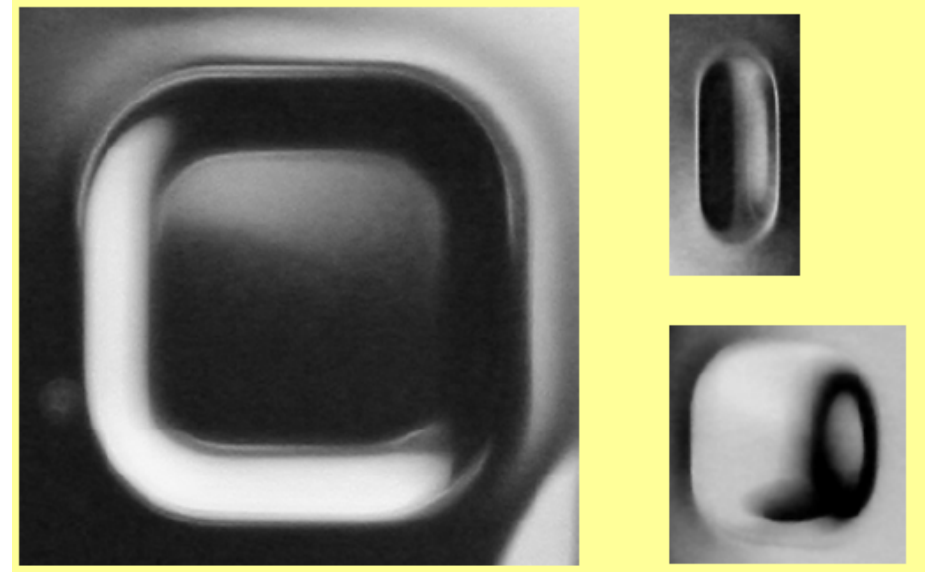
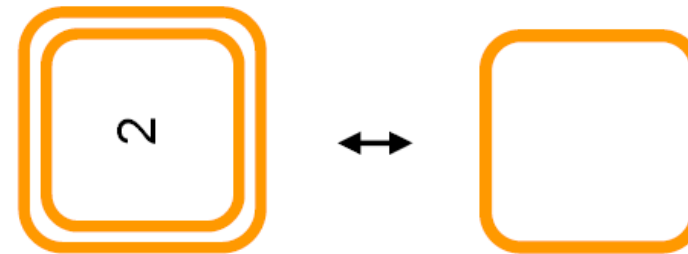
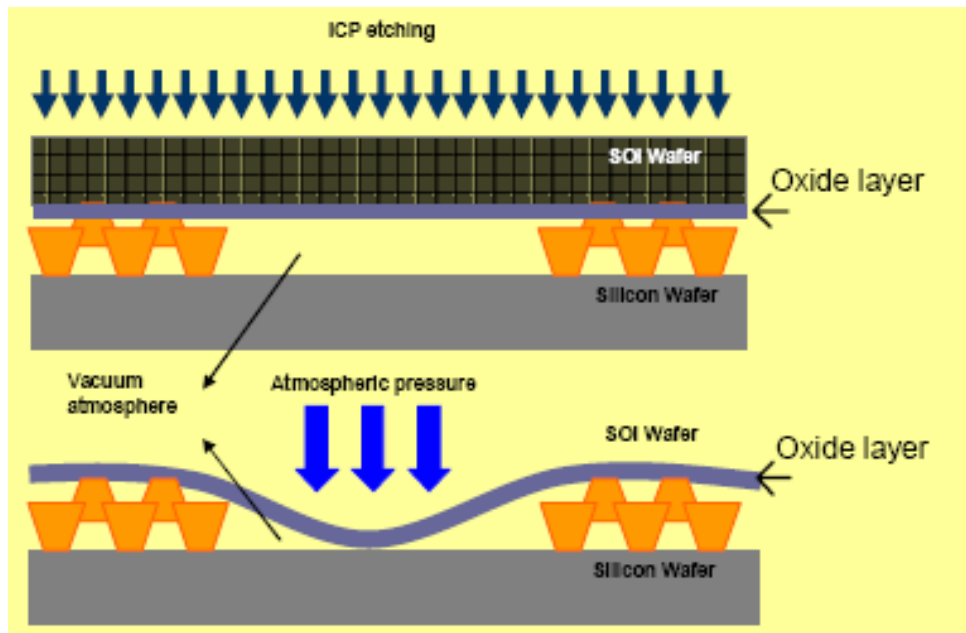
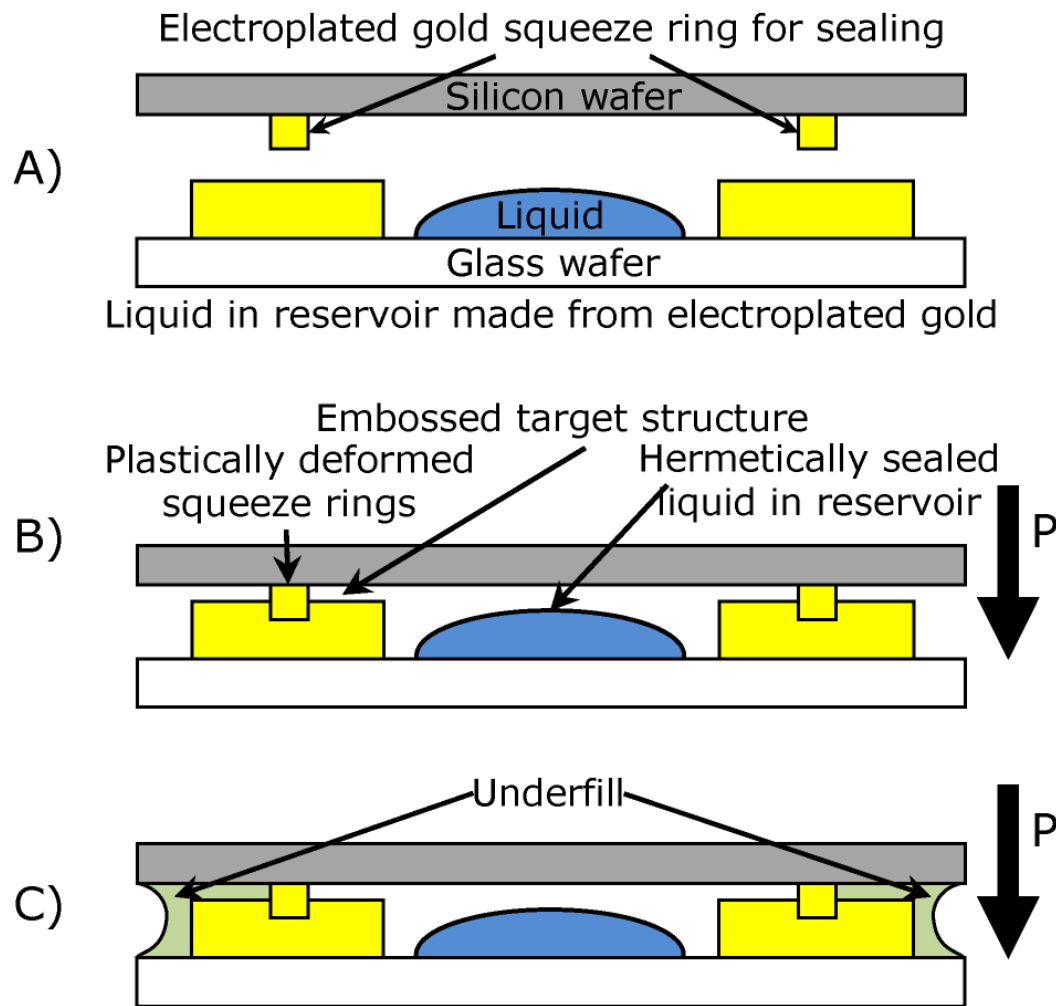


Image source: Decharat, JMEMS 2009, KTH



# Wafer-Level Sealing of Liquids Using Cold Metal Welding



- Target structures providing deformable metal surface
- Bond force  $>$  yield strength of squeeze rings  $\rightarrow$  plastic deformation
- Underfill application for mechanical stabilization

Image source: Lapis, Proc MEMS 2009, KTH



# Experimental Results

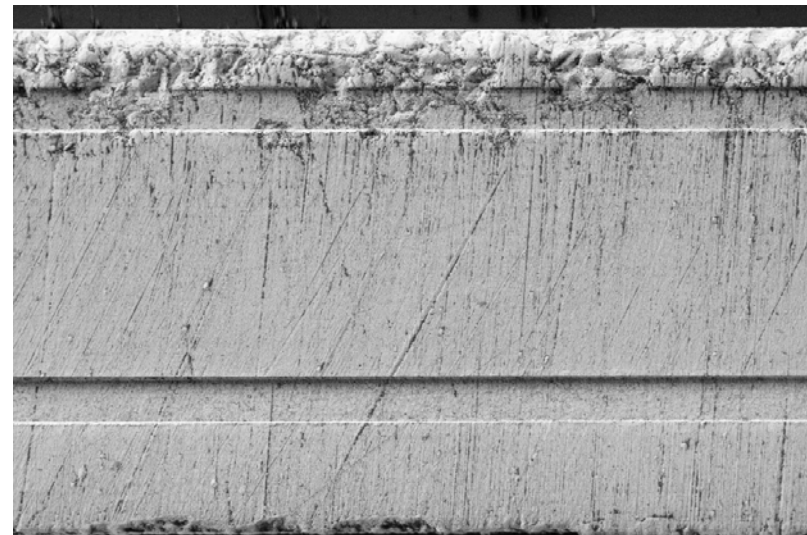
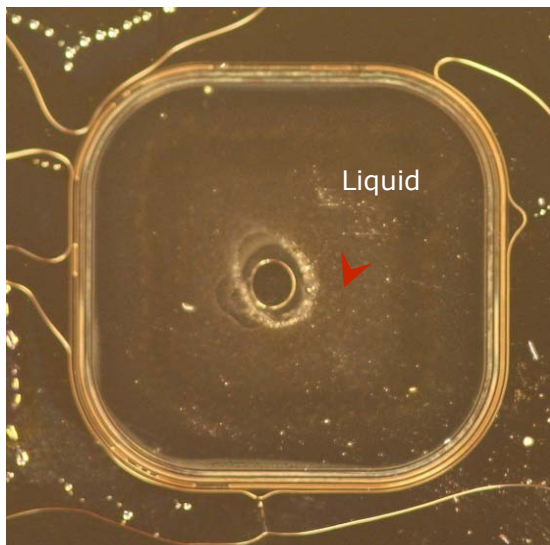
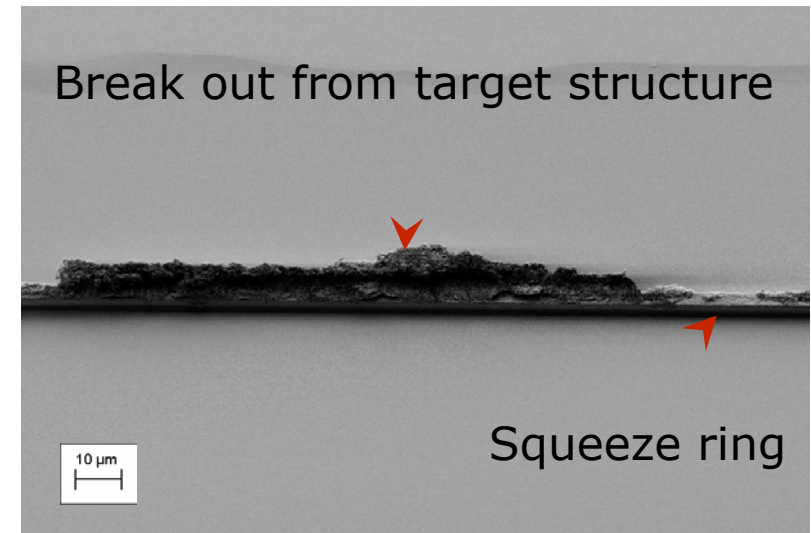
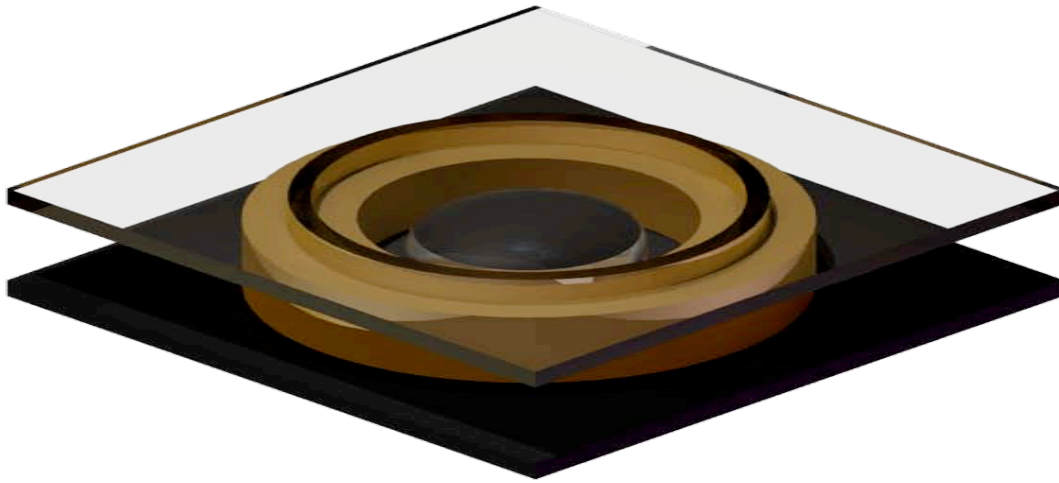
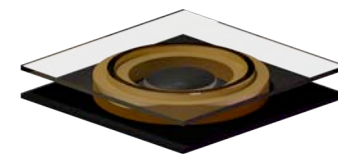
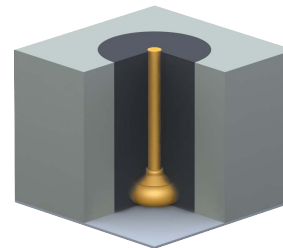
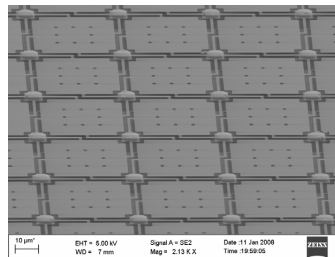
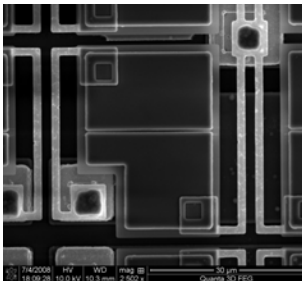


Image source: Lapisa, Proc MEMS 2009, KTH

# Summary

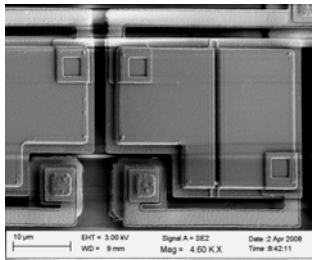
- SOIC integration platform has been implemented for IR bolometers, micro-mirrors and RF-MEMS devices and is also attractive for other IC integrated sensors.
- A new through-silicon via (TSV) platforms with wire bonded metal cores and magnet self assembly have been developed.
- Cold metal welding has been developed for wafer-level and CMOS compatible sealing of vacuum and liquids.



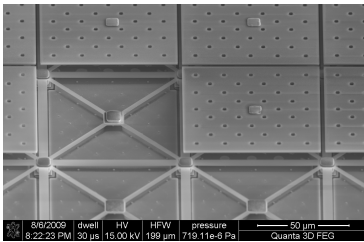
# Thank You For Your Attention!



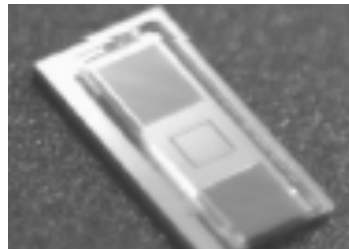
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m-SiGe on CMOS



m-Si on CMOS



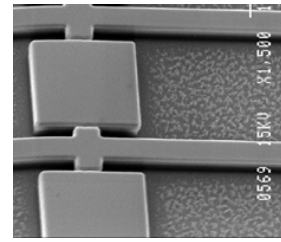
Glass on Si



PZT on Si



SMA on Si



GaAs on Si