Massive parallel EB exposure systems

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N.Ikegami (Tokyo Univ. of Agriculture and Technology))

1. Introduction
2. Parallel EB exposure systems under development in Europe and USA
3. Massive parallel EB exposure systems in this project

Appendix : Research on the parallel EB exposure systems in Tohoku University in the past

Feb.10, 2010

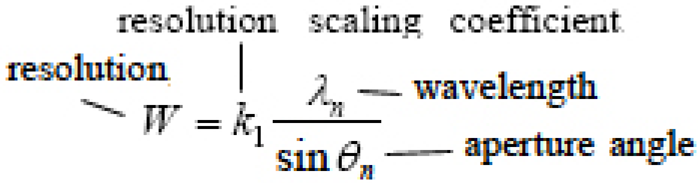
Mask cost crisis in production of advanced LSI

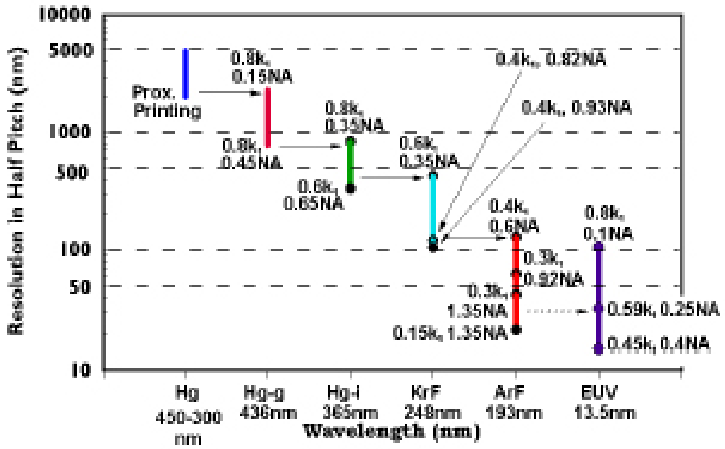
Mask-less lithography is needed for

Short turn around LSI development.

Small volume LSI production

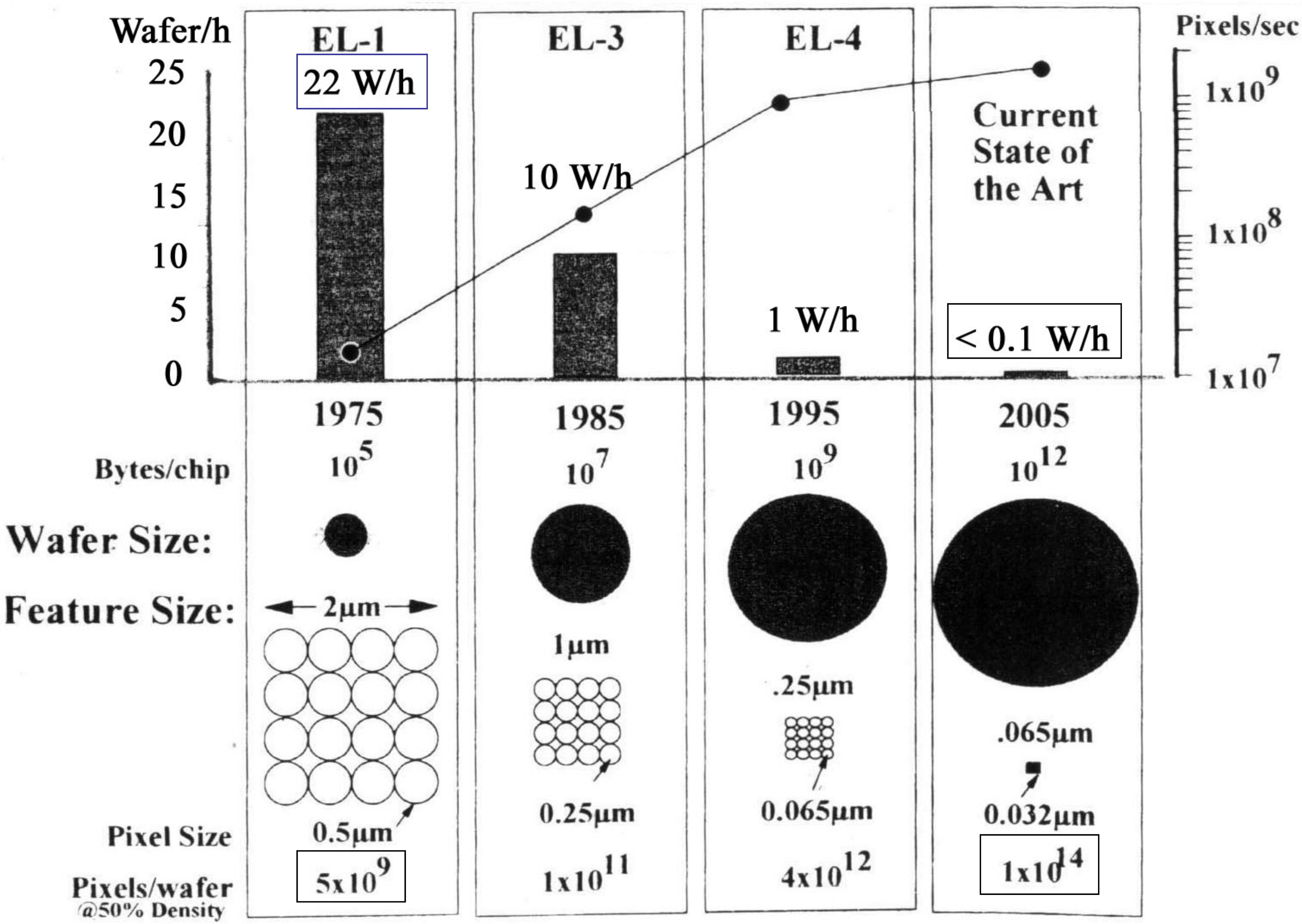
Feature size	Cost per mask set
130nm	0.3-0.4 Million US$
90nm	1 Million US$
65nm	2 Million US$
45nm	4 Million US$.



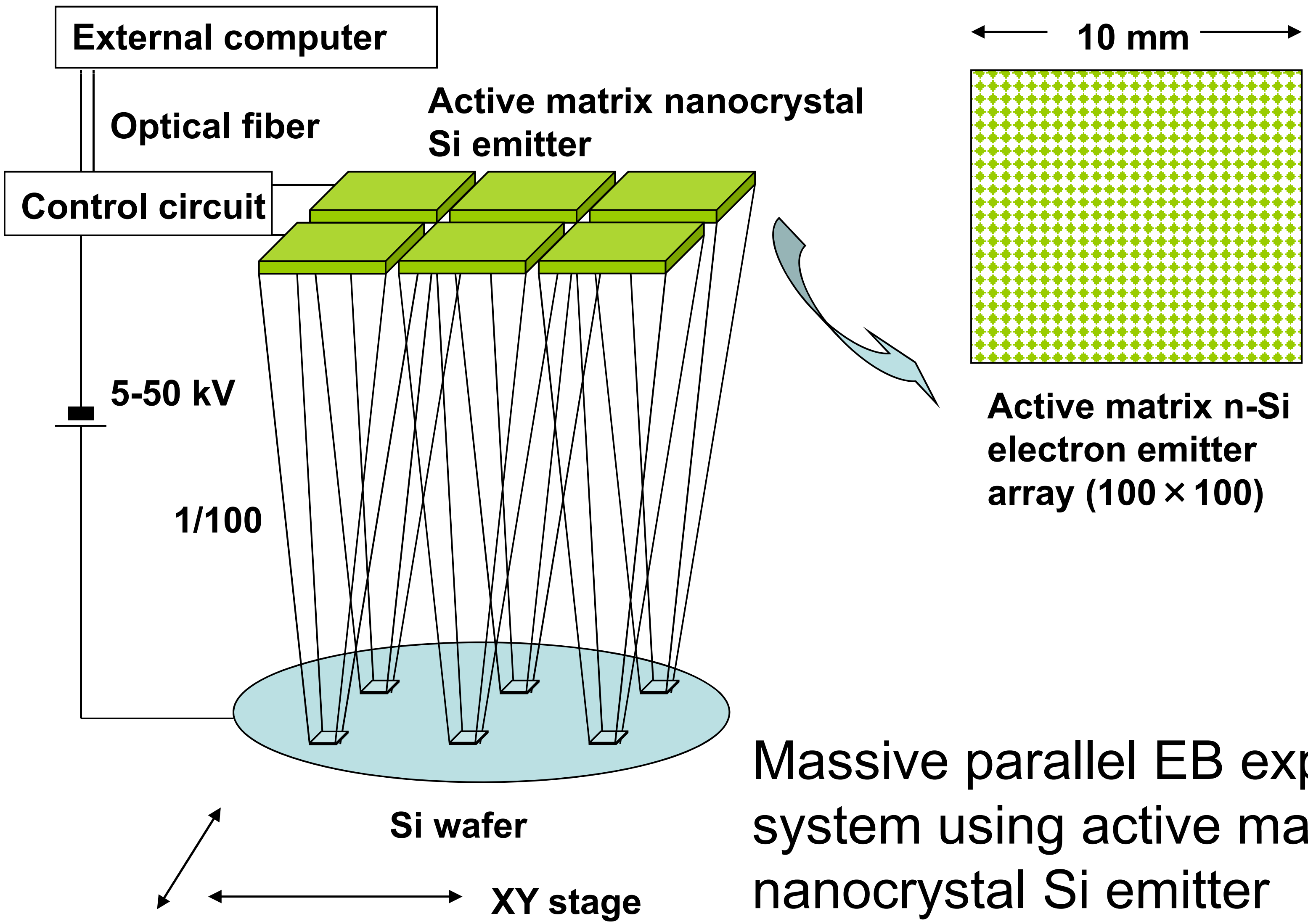


Progress of semiconductor lithography

(B.J.Lin, MEMS 2010, p.1)



Thoughput of EB lithography (H.Arimoto (Selete), Seminar of Electronic Journal (2005) 11)



Massive parallel EB exposure system using active matrix nanocrystal Si emitter

(collaborators : A Kojima & H. Ohyi (Crestec corp.), Prof. N.Koshida (Tokyo Univ. of Agriculture and Technology))

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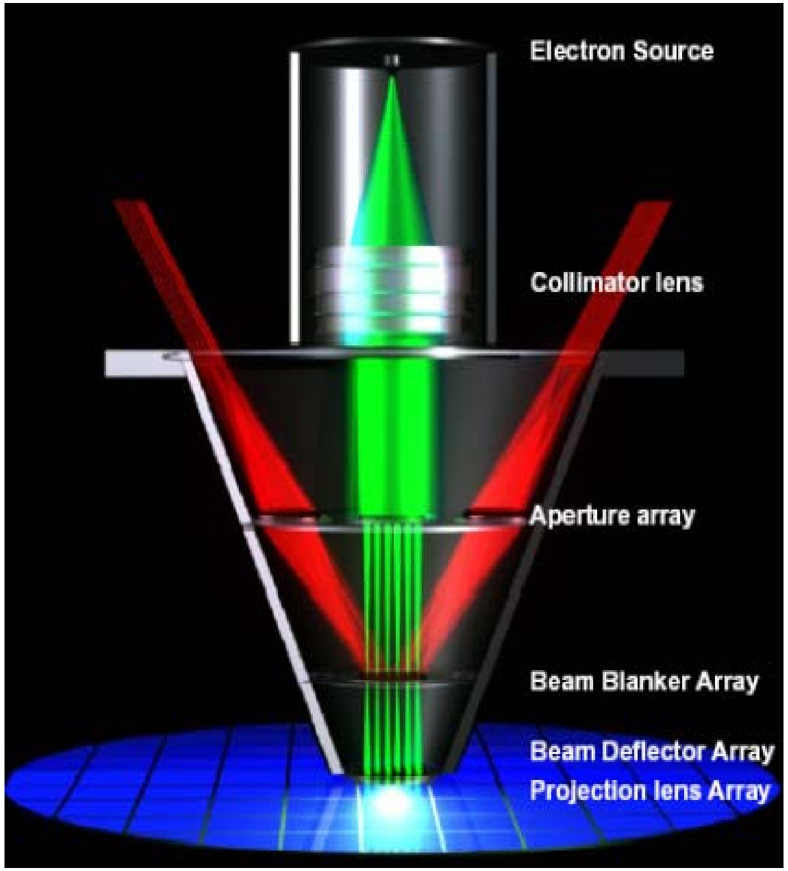
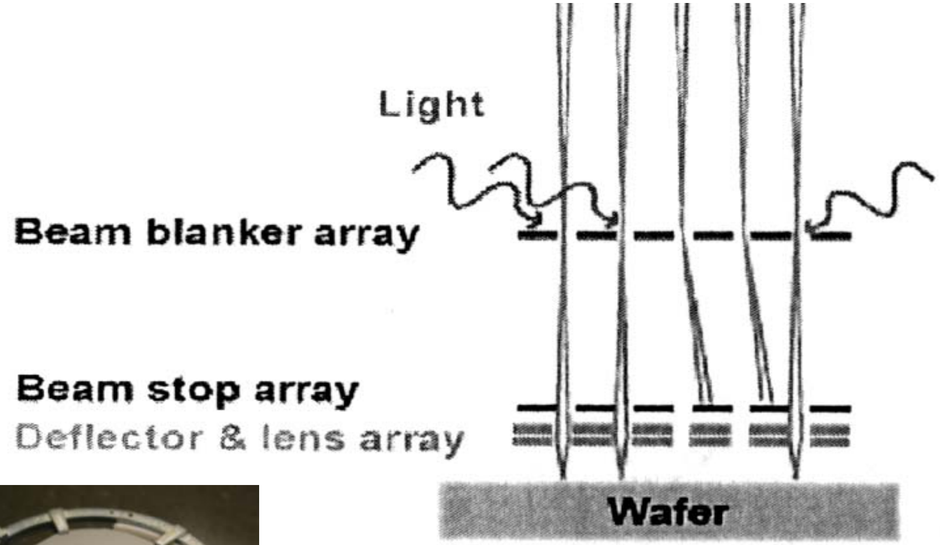
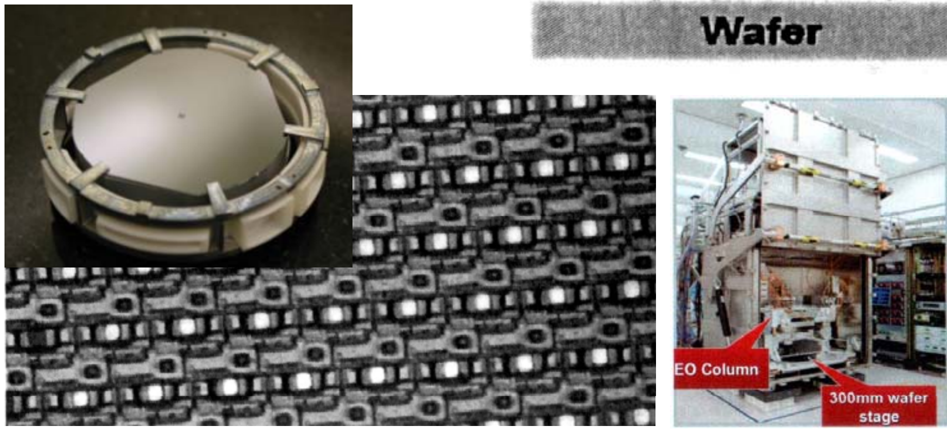






10 wafers (300mm) / hour, 110 beams → 13000 beams, , Acceleration 5kV (low)
Beam diameter 22nm (resolution 30nm), Beam current : 0.3nA

Y direction : electronic deflection in 2μm、X direction : stage scan

MAPPER (Multiple Aperture Pixel by Pixel Enhancement of Resolution) (The Netherlands)

(http://www.mapperlithography.com/, B.J.Kampherbeek, Maskless meeting, San Jose (2005))

Most forms of high throughput charged particle beam lithography (shaped beam, Gaussian beam, cell projection,[1] mask projection[2] as in SCALPEL,[3] or ion projection[4]) are ultimately limited by stochastic Coulomb interactions between individual particles in the beam. There are two exceptions. The first is a 1:1 photomask image projection,[5] a technique developed between 1975 and 1985 mainly in Japan and the U.K. However, this technique has serious mask problems: it is a 1:1 mask and the photo cathode is very sensitive to contamination. The second is multimicrocolumn lithography,[6] developed between 1985 and 1995 at IBM. However, as far as I know, the question of how to control a large number of minicolumns has not yet been answered. In the present proposal some aspects of both the 1:1 image projection and the minicolumn approach will be incorporated.

Structured metal–insulator-metal (MIM) or metal–oxide–semiconductor (MOS) cathodes have been proposed for use in lithography. One of the problems is that if the cathode is damaged even at one pixel, it is useless. Also, it is difficult to get homogeneous emission. Using a scheme similar to Fig. 3, it should be possible to make an array of small MIM or MOS cathodes for the MAPPER machine.

Conventional EB system
→ Beam spread by coulomb interaction

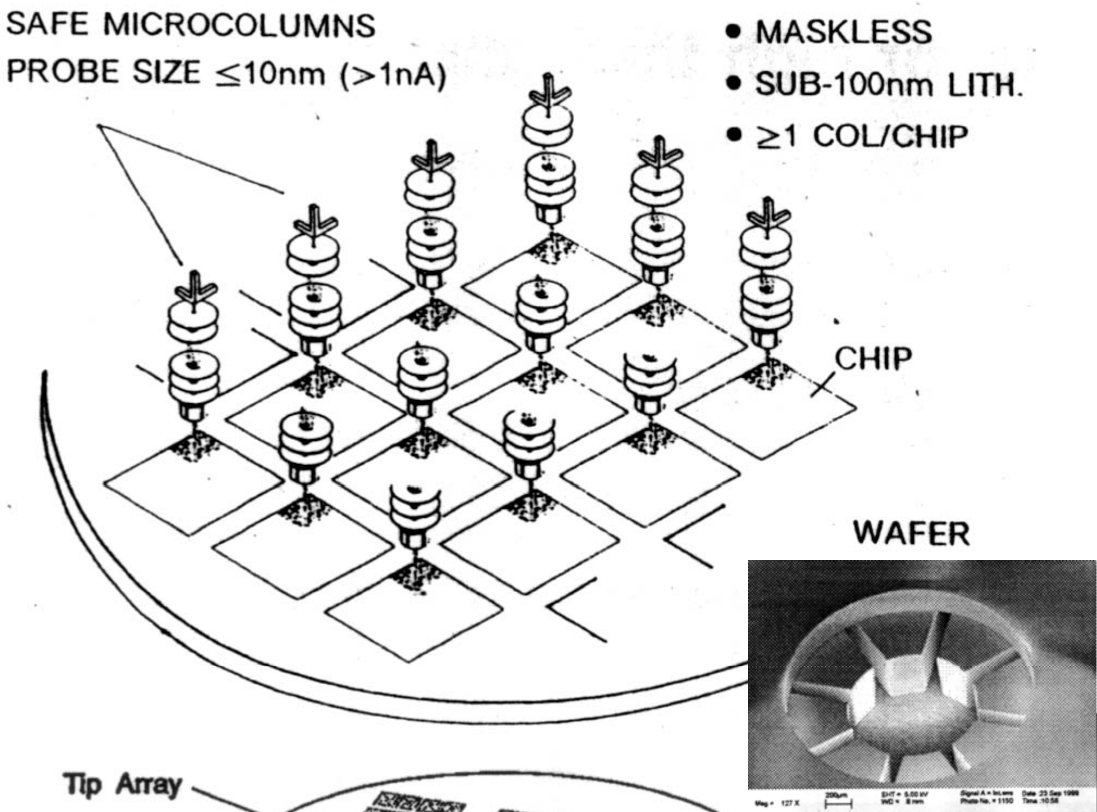
1:1 projection
→ Mask problems

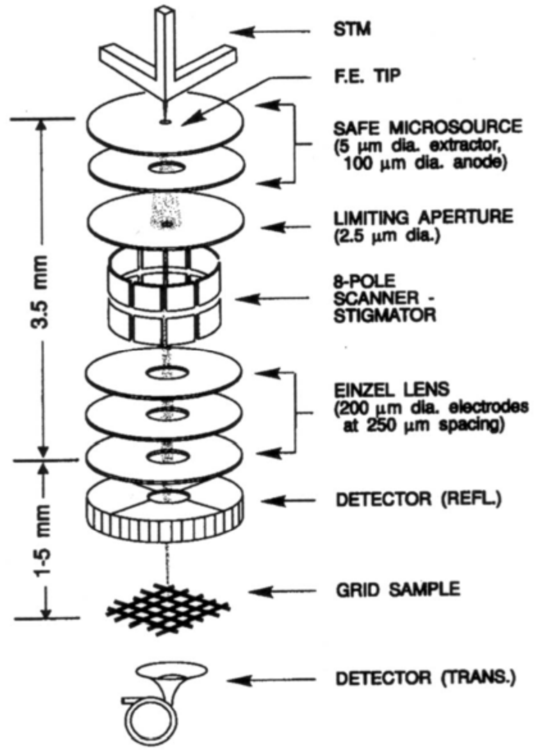
Multi-column
→ Complexity of control

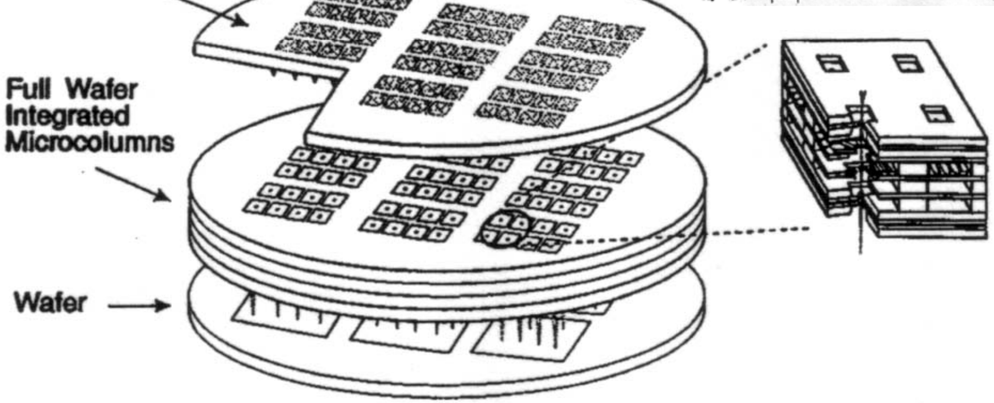
Areal electron source
→ Dispersion of electron emission

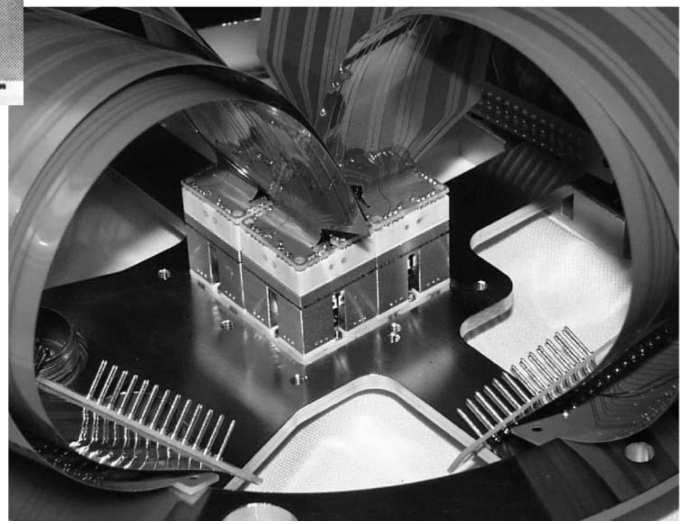
Problems

(P.Kruit (Mapper), J.Vac.Sci. Technol., B 16 (1998) 3177)



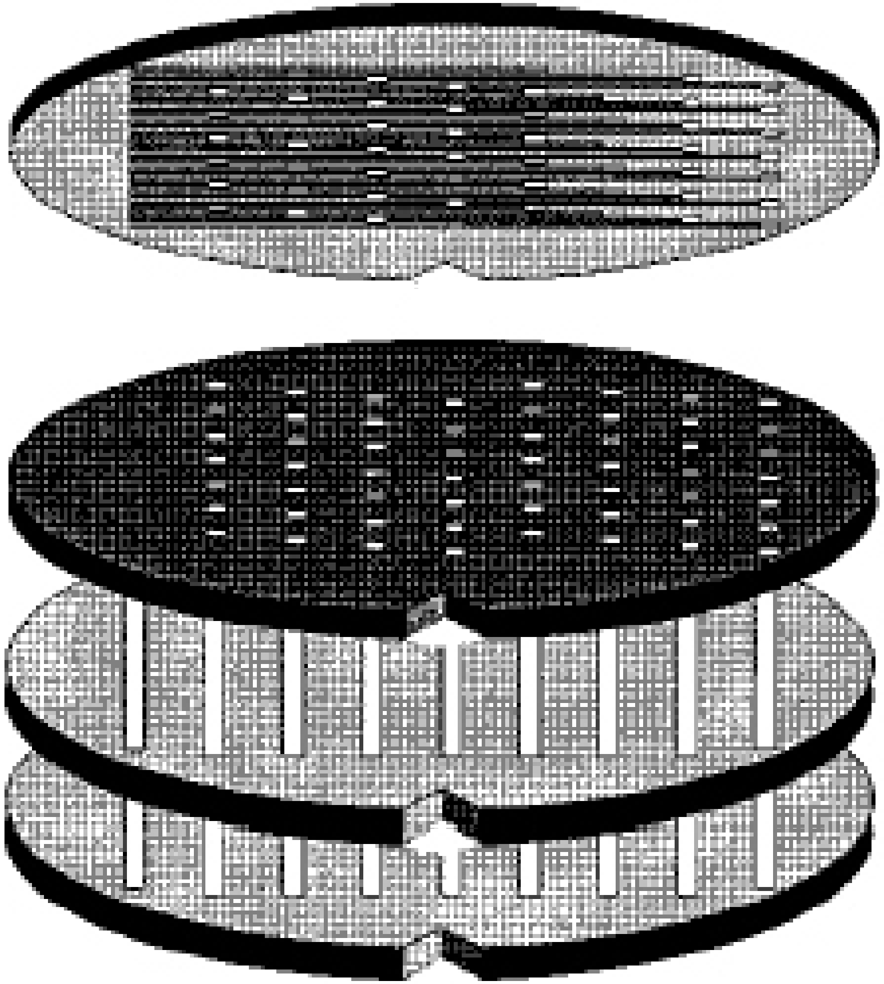






Microcolumn arrays (1kV) ⑧

(T.H.P.Chang (IBM → Etec, Applied Materials), Microelectronic Eng., 57-58 (2001), p.117)



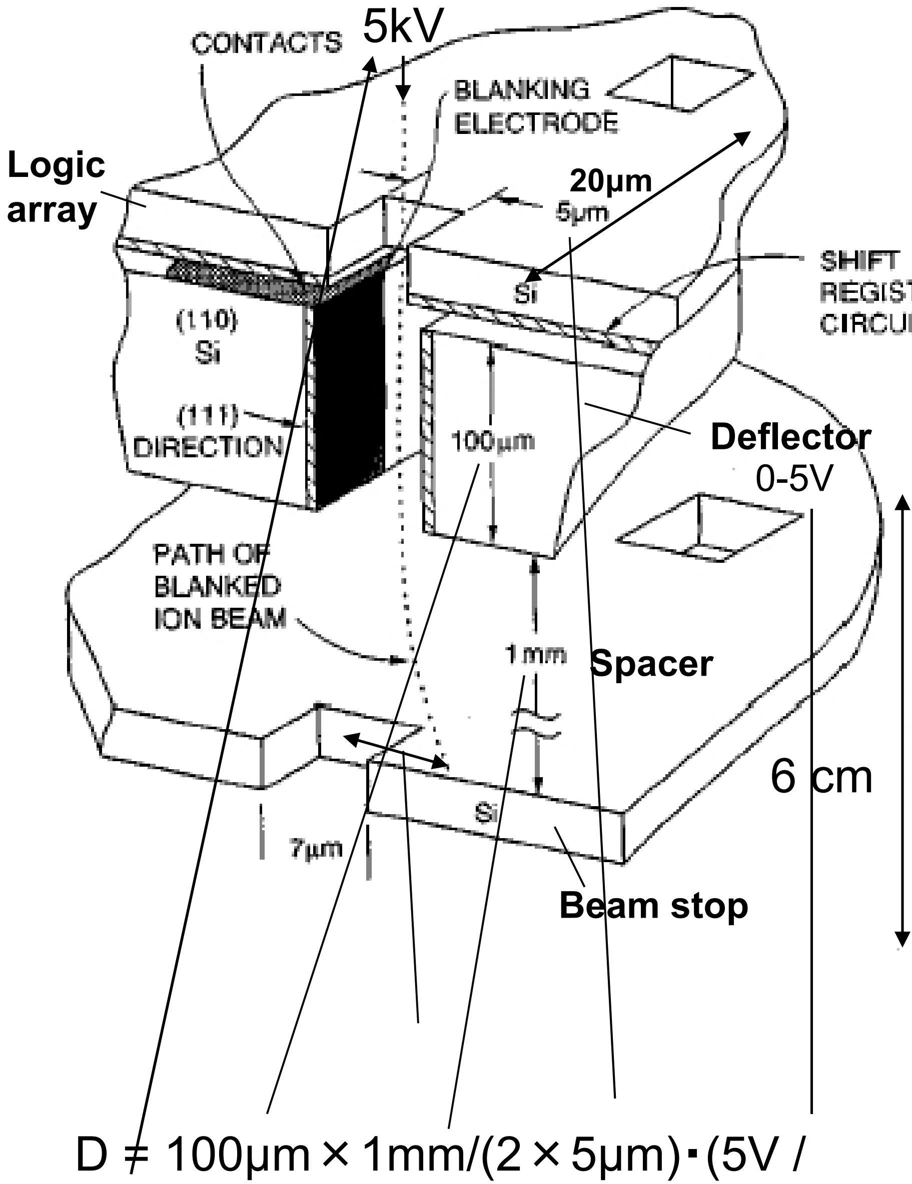
Logic array, Contains 3000 x 3000 array of apertures, each aperture is connected through a 4 bit shift register to it's neighboring aperture to the left.   This wafer is flip-chip bonded to deflector plate.

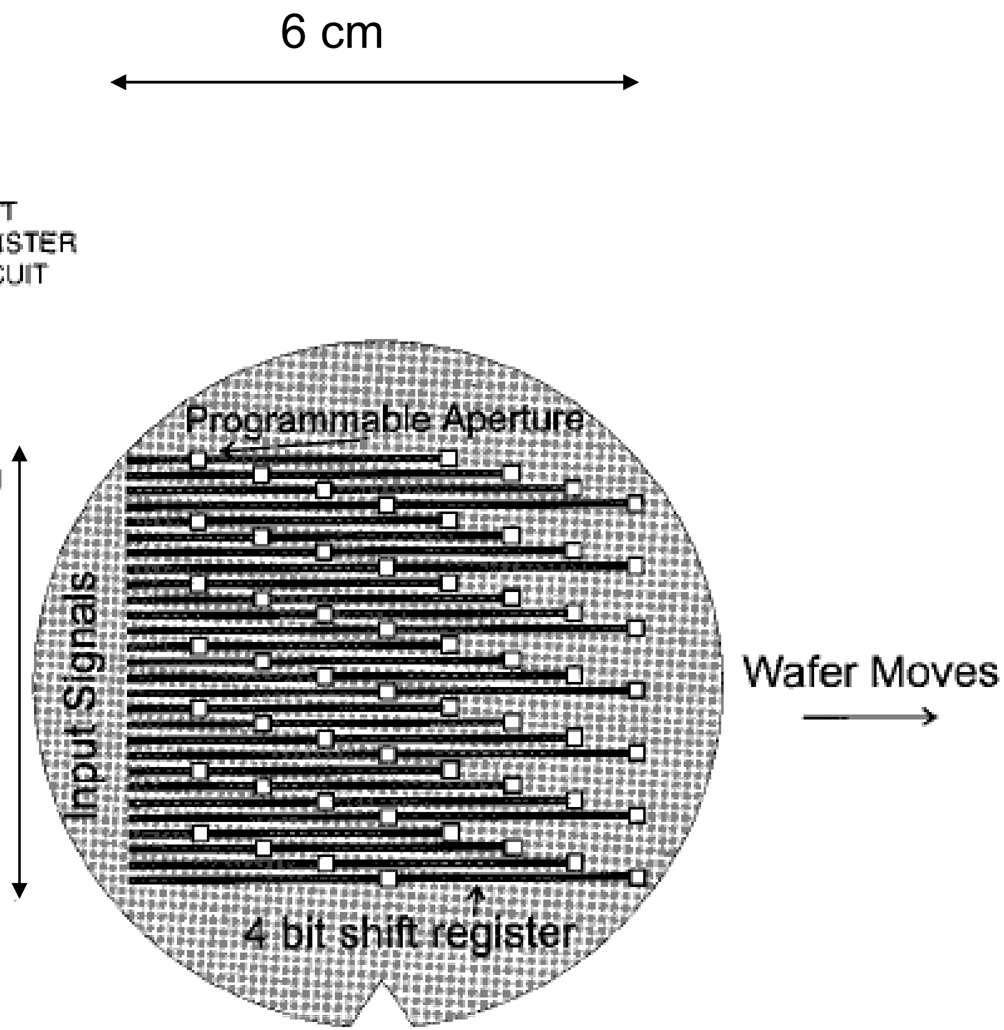
Deflectors, Made using LIGA process, thinned to 100µm.

Spacer, <110> anisotropically etched, 7µm wide groves

Beam Stop, <110> anisotropically etched, 7µm wide groves

(I.Berry (Microel. Res. Lab. Columbia), J.Vac.Sci.Tec. B, 15 (1997) 2382)

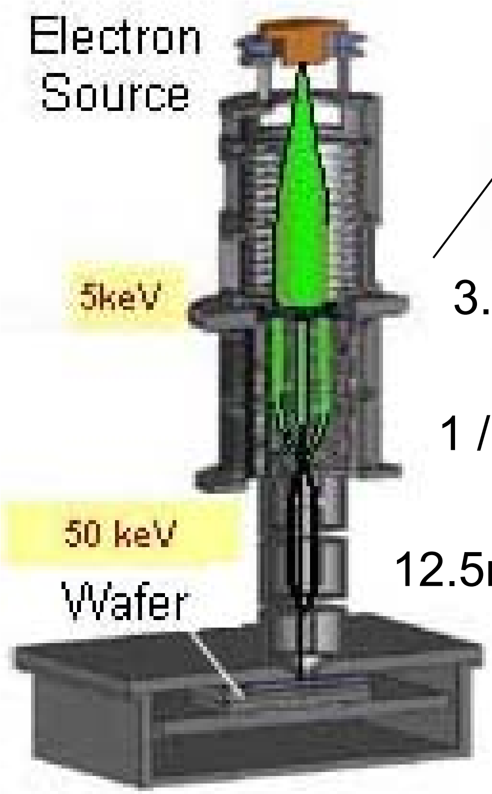




実際は 3000×3000

D = 100μm×1mm/(2×5μm)･(5V / 5kV) = 10μm

(I.Berry (Microel. Res. Lab. Columbia), J.Vac.Sci.Tec. B, 15 (1997) 2382)

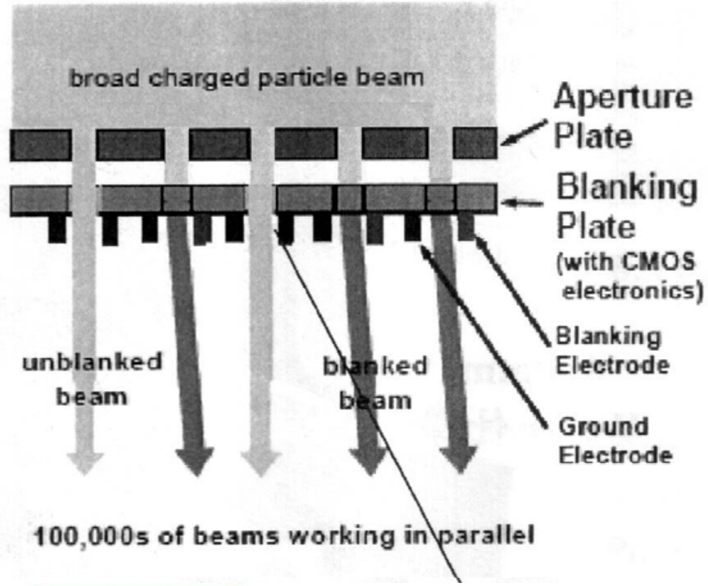


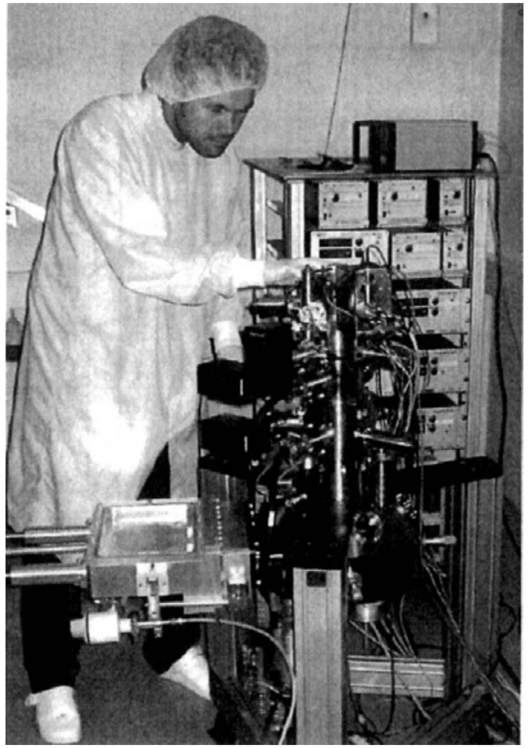
3.5µm

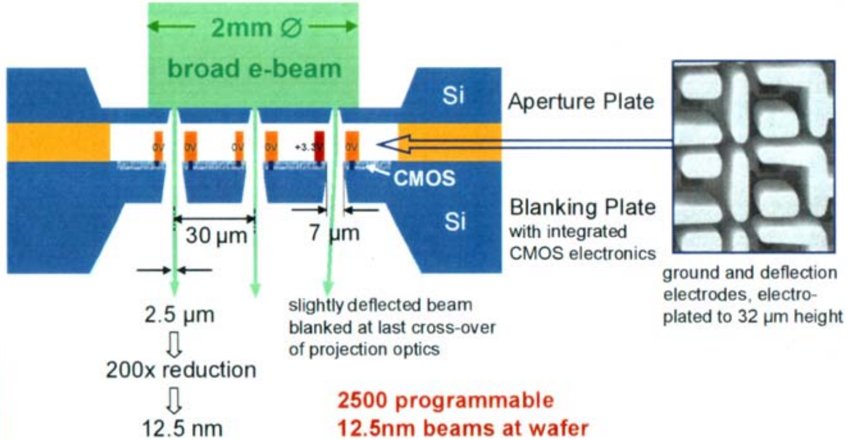
1 / 200

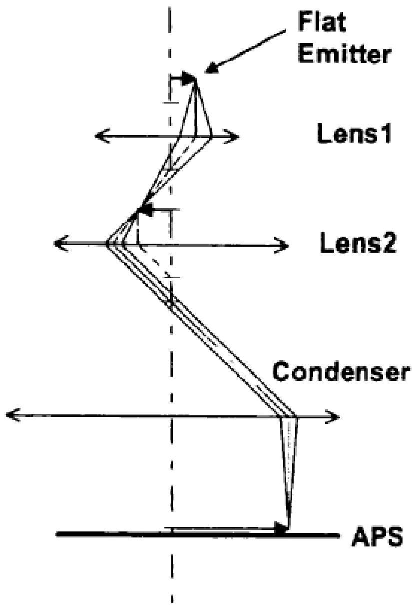
12.5nm

APS (Aperture Plate System)









Single electron source
→ beam uniformity

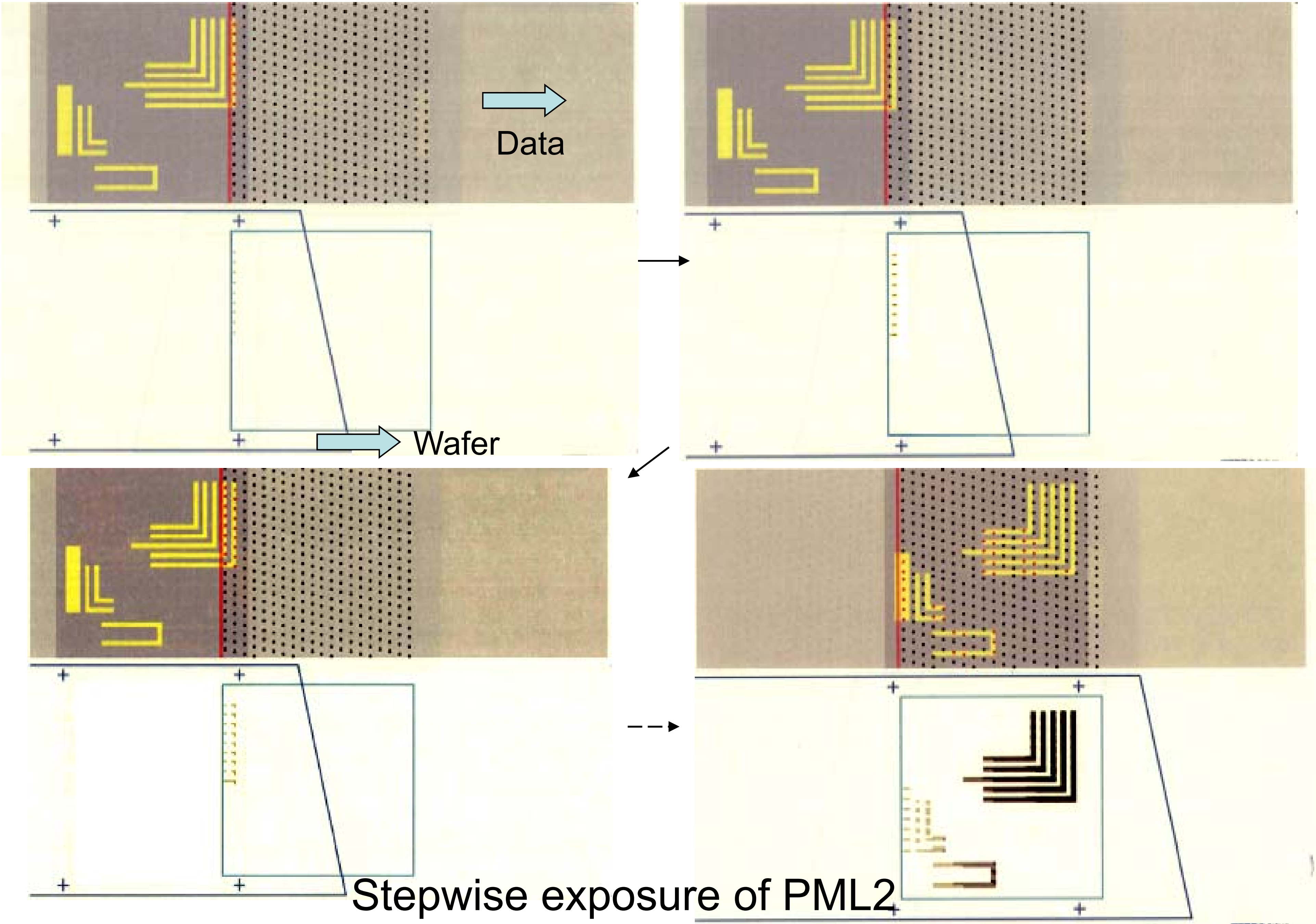
High voltage (50kV) and
large reduction ratio (1/200)
→ high resolution (12.5nm)

Low 1st stage voltage (5kV)
→ low damage to APS and
high speed blanking

(C.Klein, Proc.SPIE, 7637 (2010) 76370B)

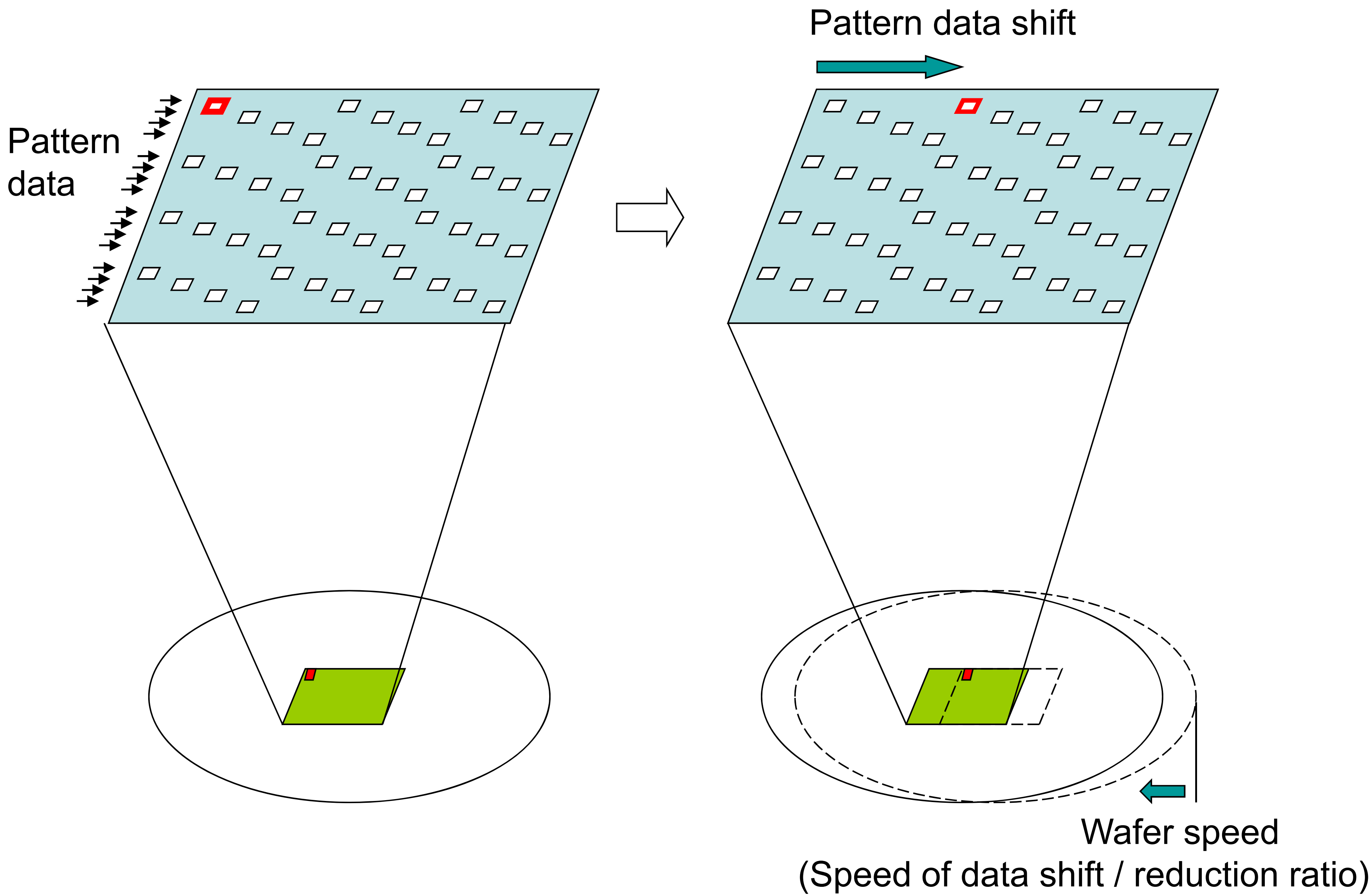
PML2 : Projection Mask-Less Lithography

(IMS Nanofabrication AG (Austria))



Stepwise exposure of PML2

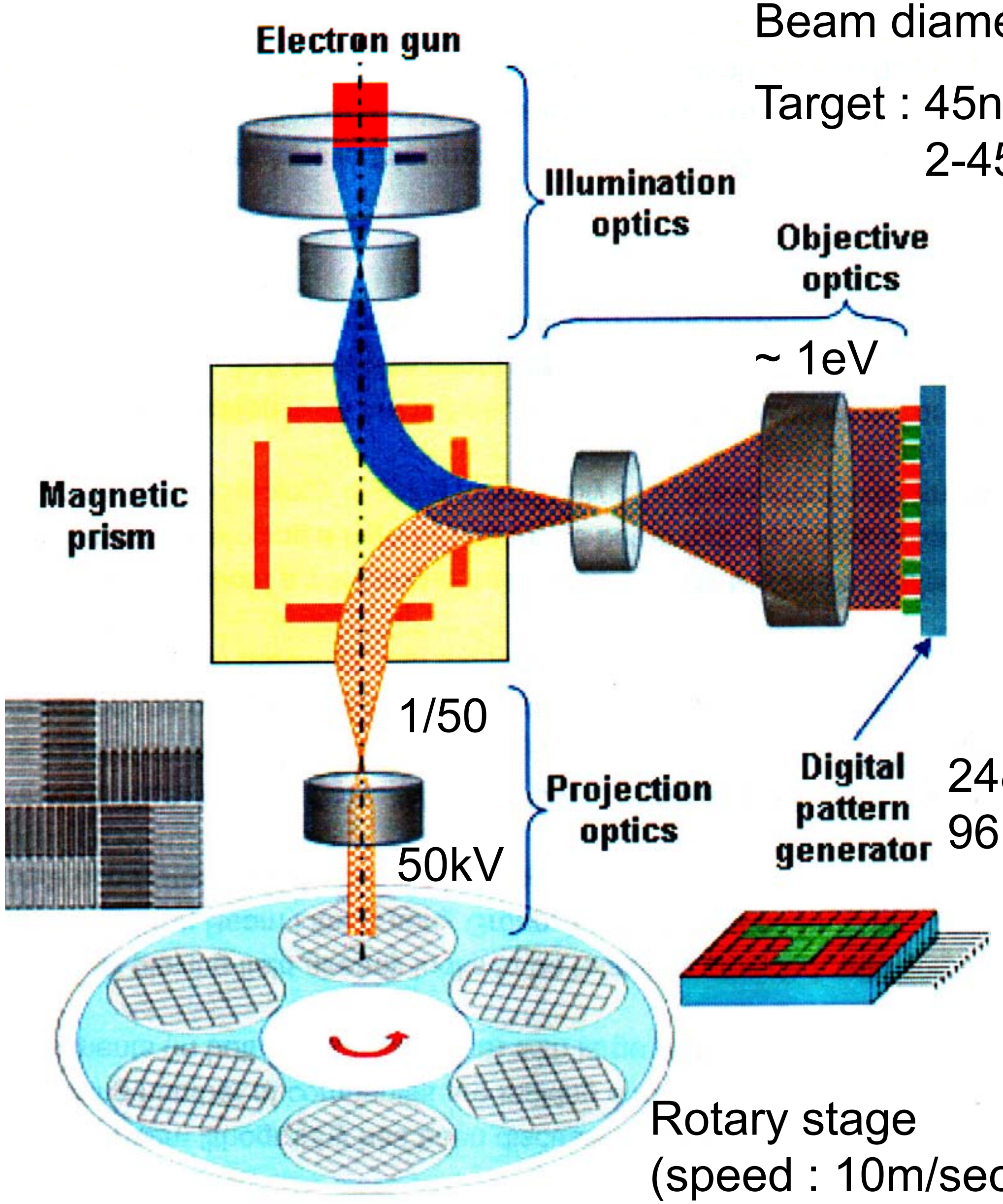
(C.Brandstatter (IMS), SEMATEC Litho Forum)



Multiple exposure using pattern data shift and wafer motion

Beam diameter : 30nm

Target : 45nm (32nm),
2-45 wafers / Hr



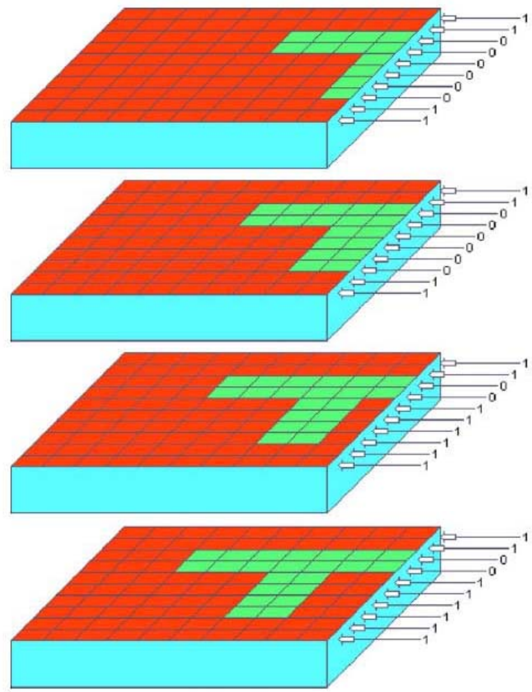
~ 1eV

1/50

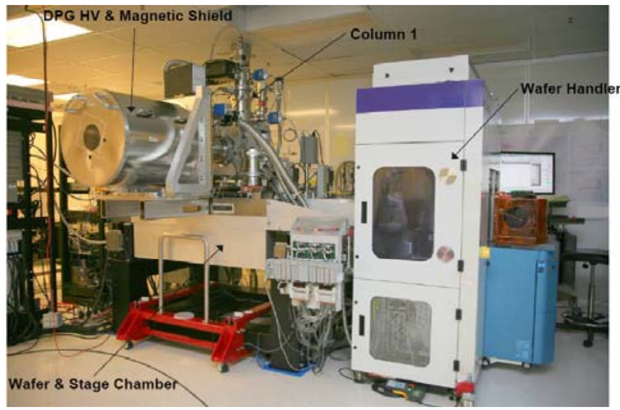
50kV

248 × 40
96 =10^6

Rotary stage
(speed : 10m/sec)

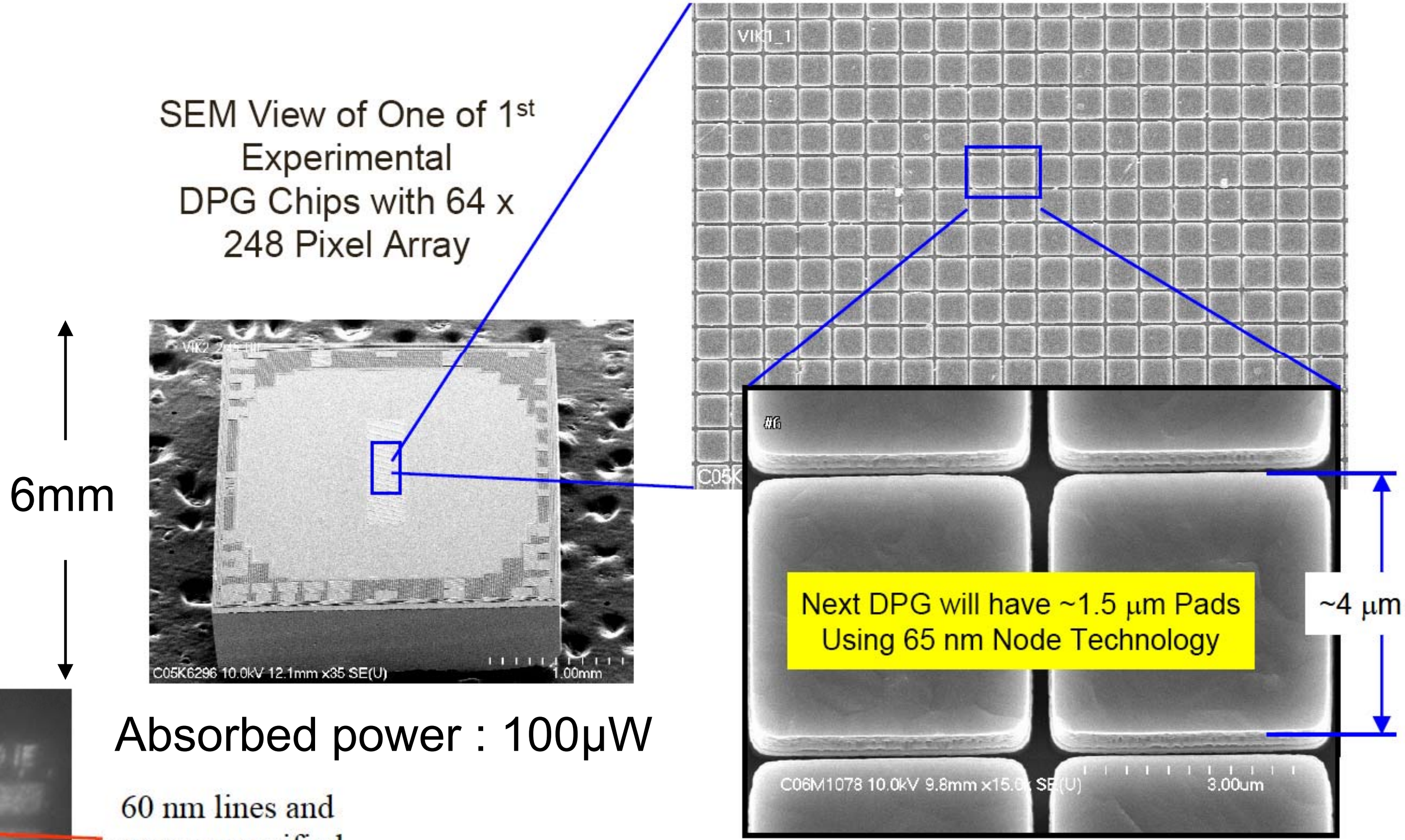


Time Domain Integration (TDI)



REBL (Reflected E-Beam Lithography) (KLA-Tencor, USA)

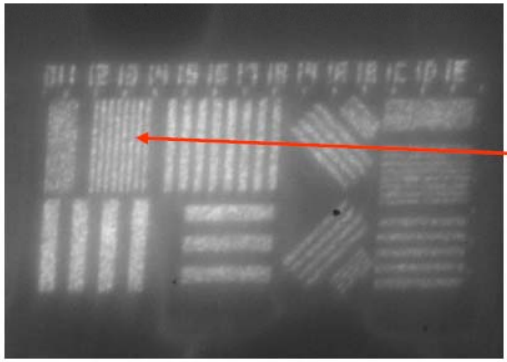
(P.Petric (KLA-Tencor), J.Vac. Sci. Tech. B, 27 (1) (2009) 161)



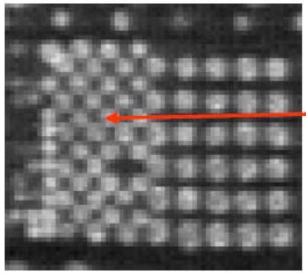
Absorbed power : 100μW

DPG (Digital Pattern Generator)

4μm / 50 = 80nm、1.5μm / 50 = 30nm



60 nm lines and spaces magnified onto scintillator screen



60nm contact holes in PMMA resist

(M.McCord (KLA-Tencor), SEMATECH Workshop on Maskless Lithography (2008))

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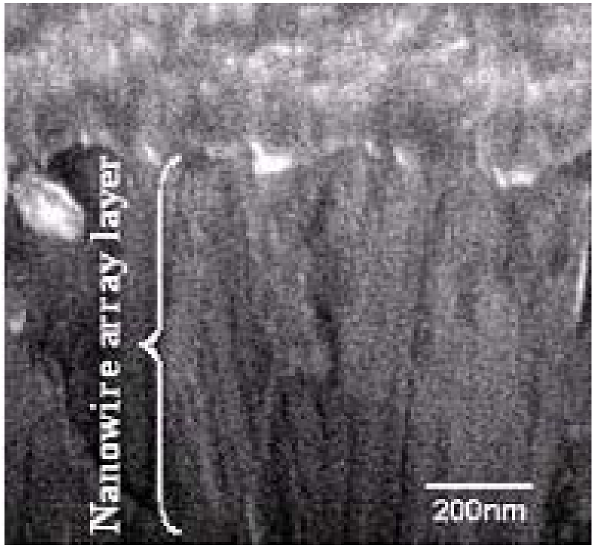
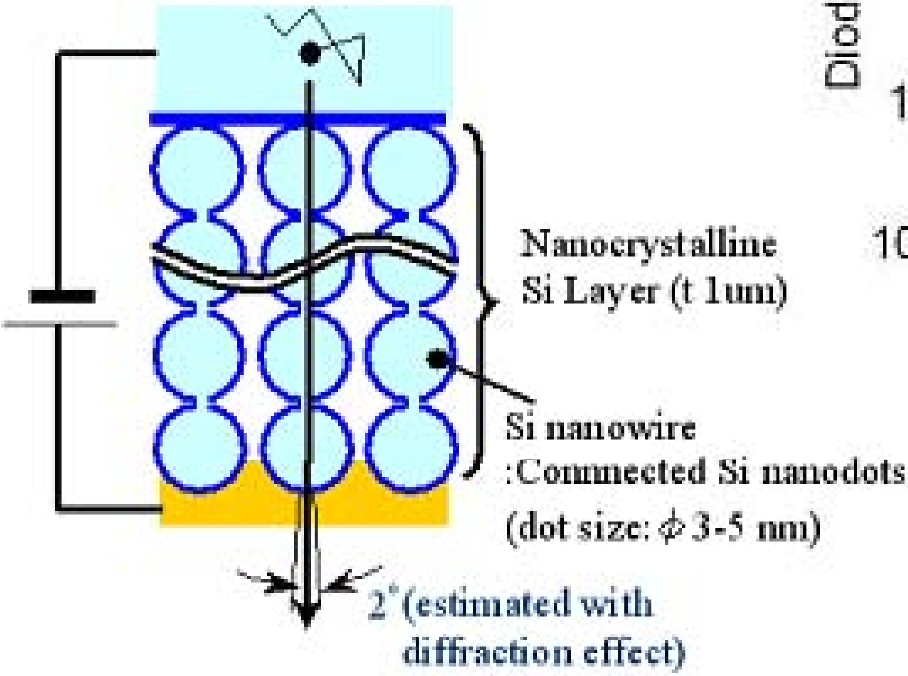
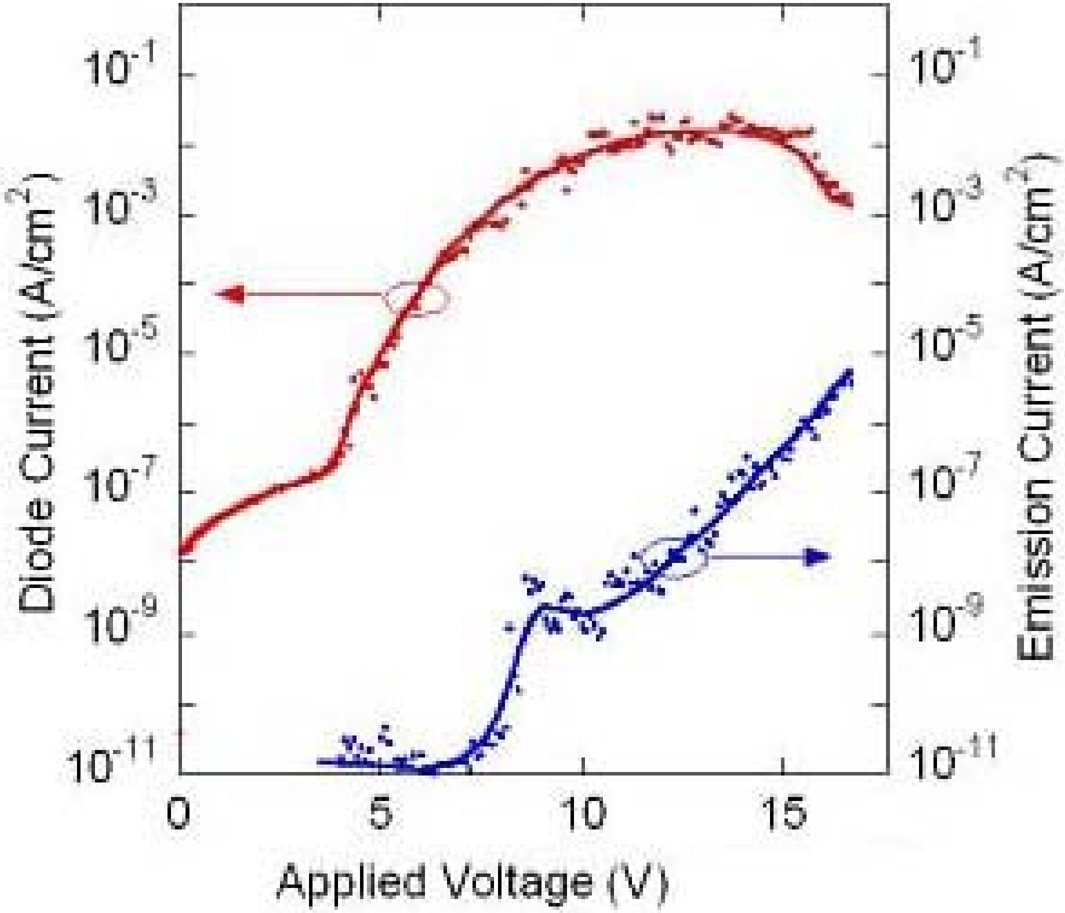


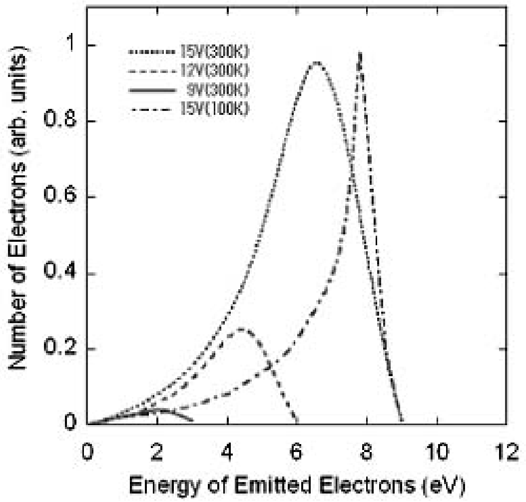




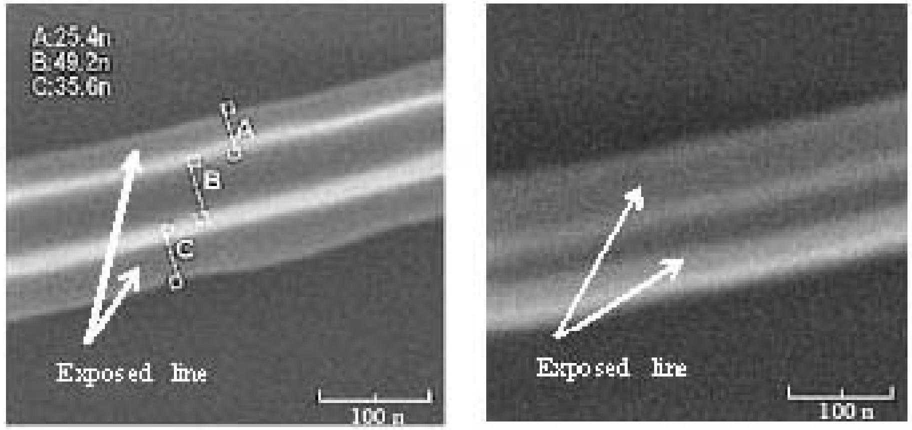
Nanocrystal Si emitter

(low control voltage → active matrix)

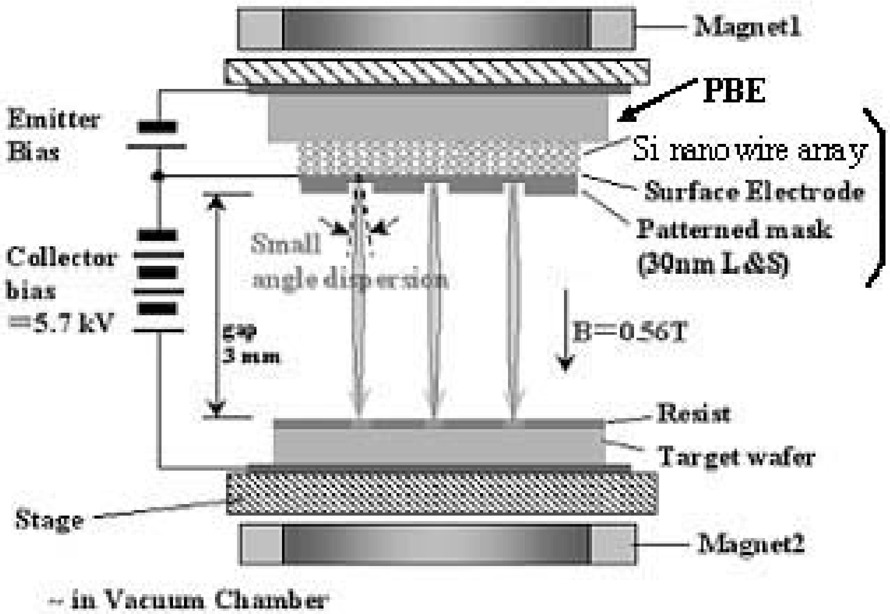
(A Kojima, H. Ohyi and N. Koshida, J. Vac. Sci. Technol., B26, 6 (2008) 2064)

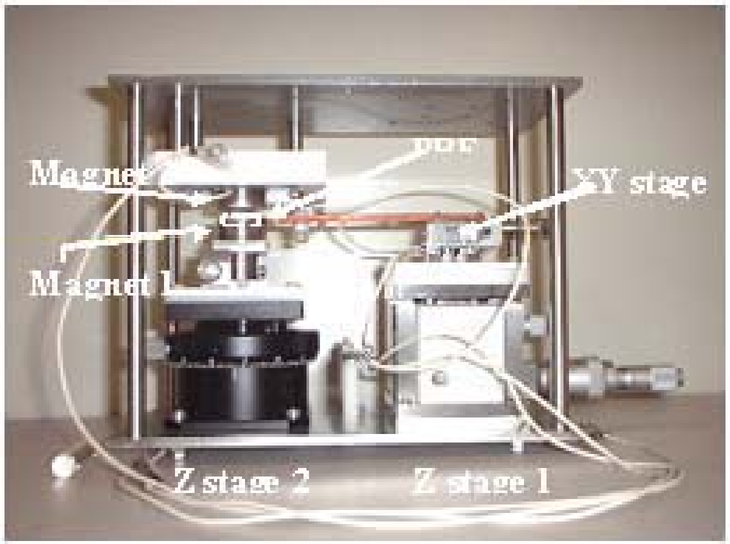


Electron energy from Nanocrystal Si electron emitter



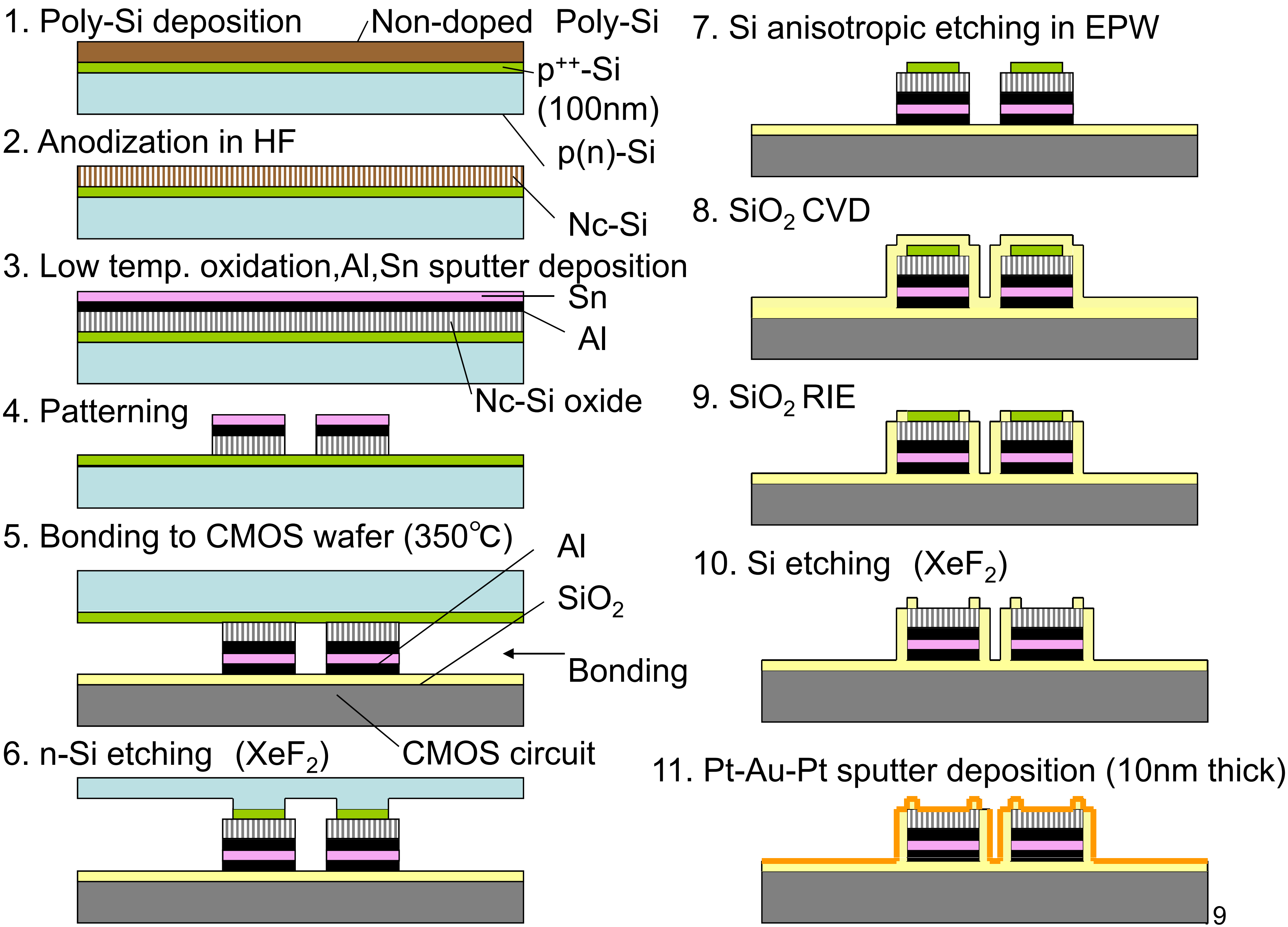
SEM images of transferred parallel lines pattern using PBE



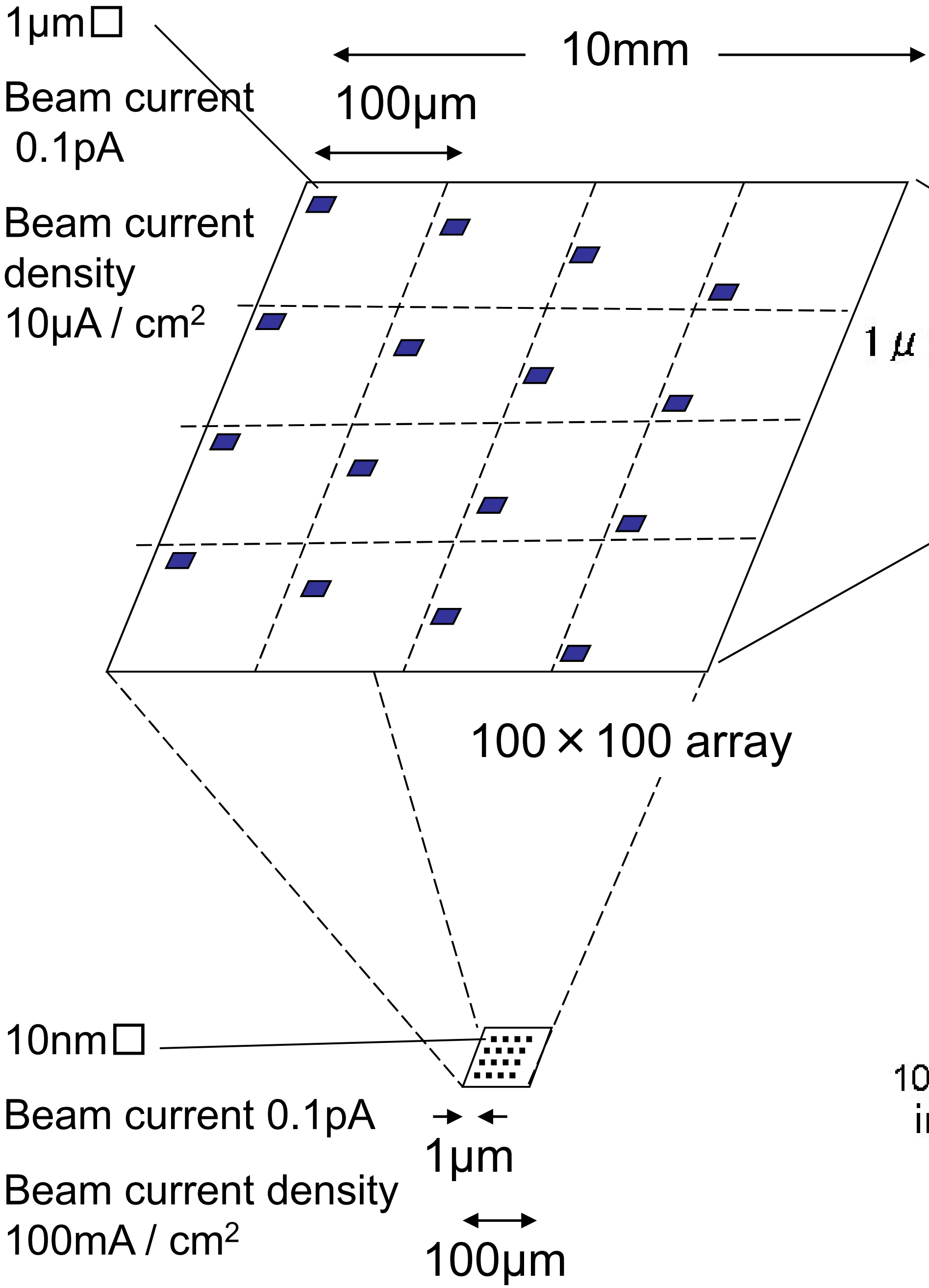


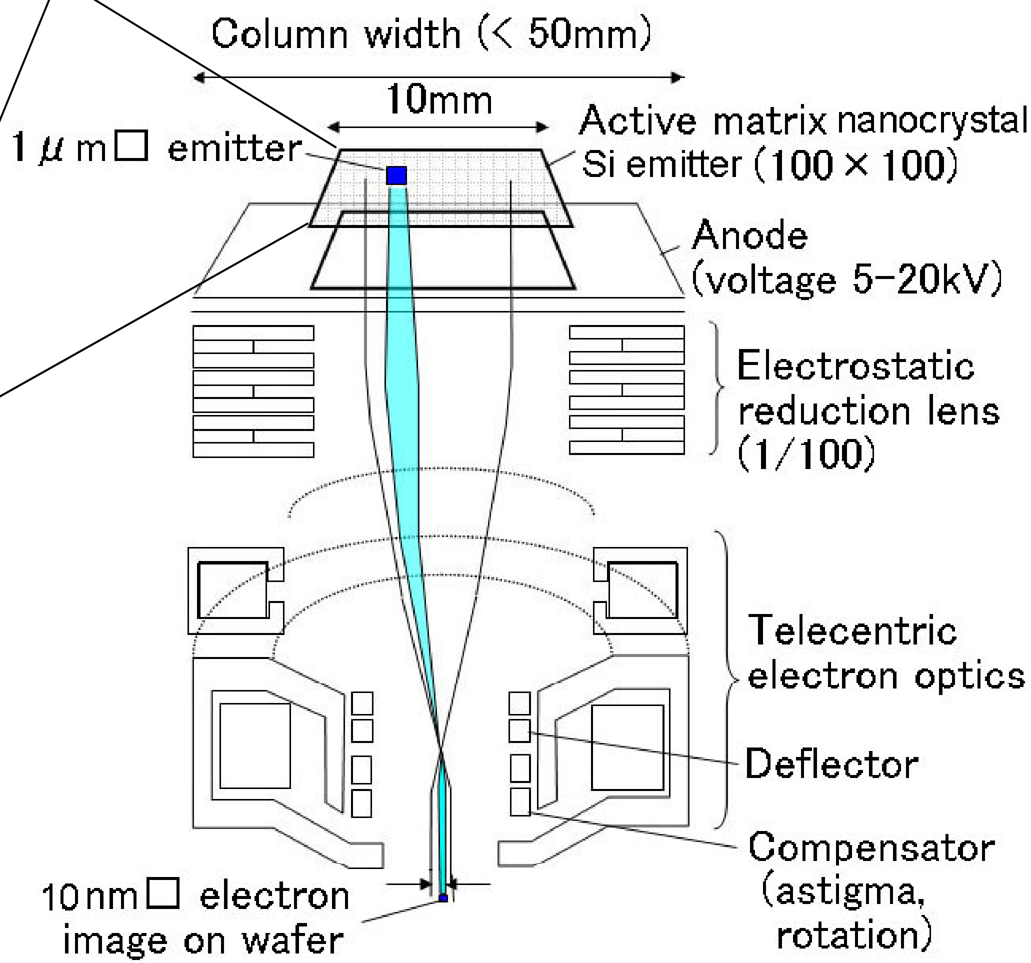
1:1 Image projection system using nanocrystal Si emitter

(A Kojima, H. Ohyi and N. Koshida, J. Vac. Sci. Technol., B26, 6 (2008) 2064)



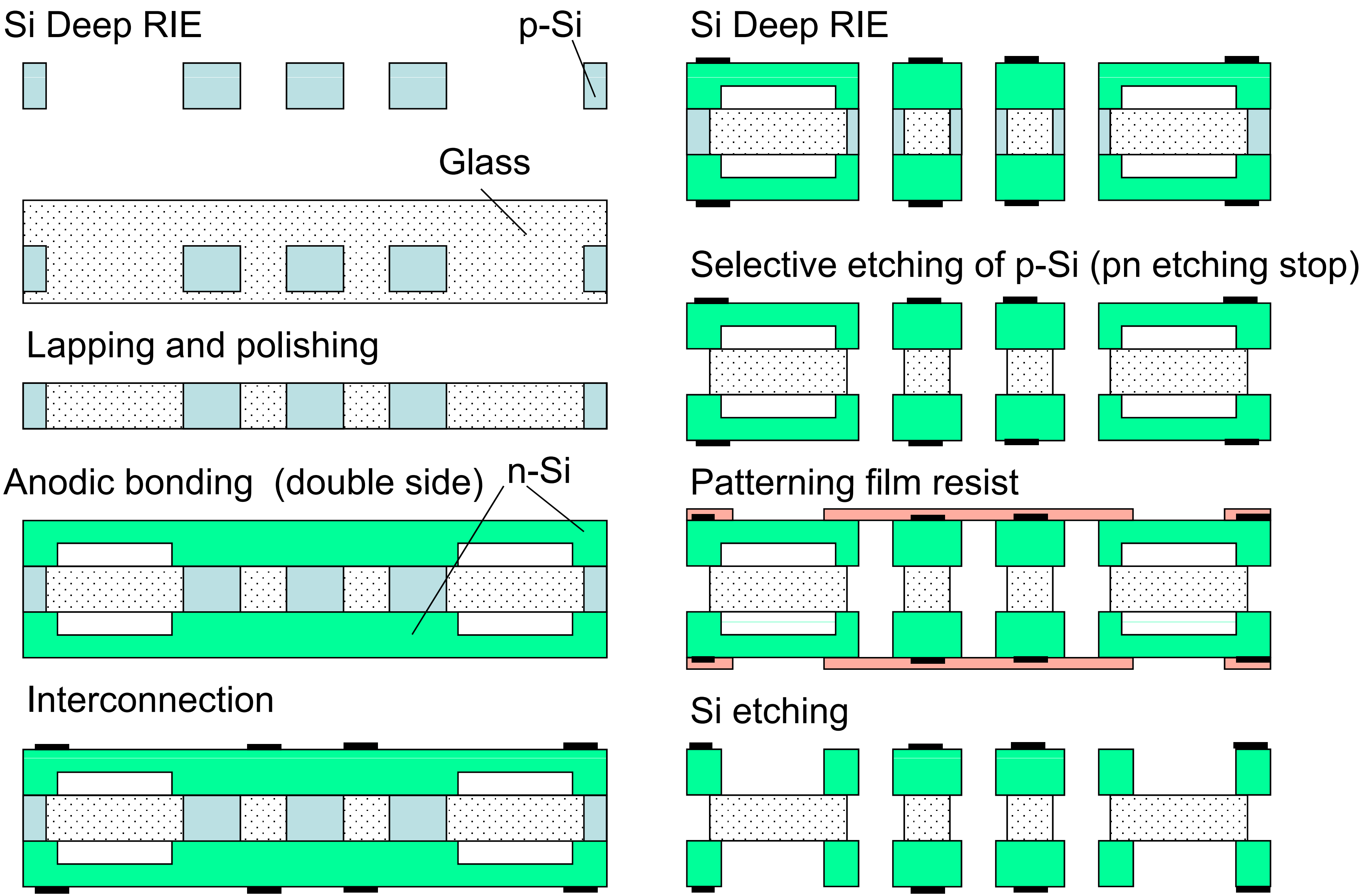
Fabrication process of nanocrystal Si emitter



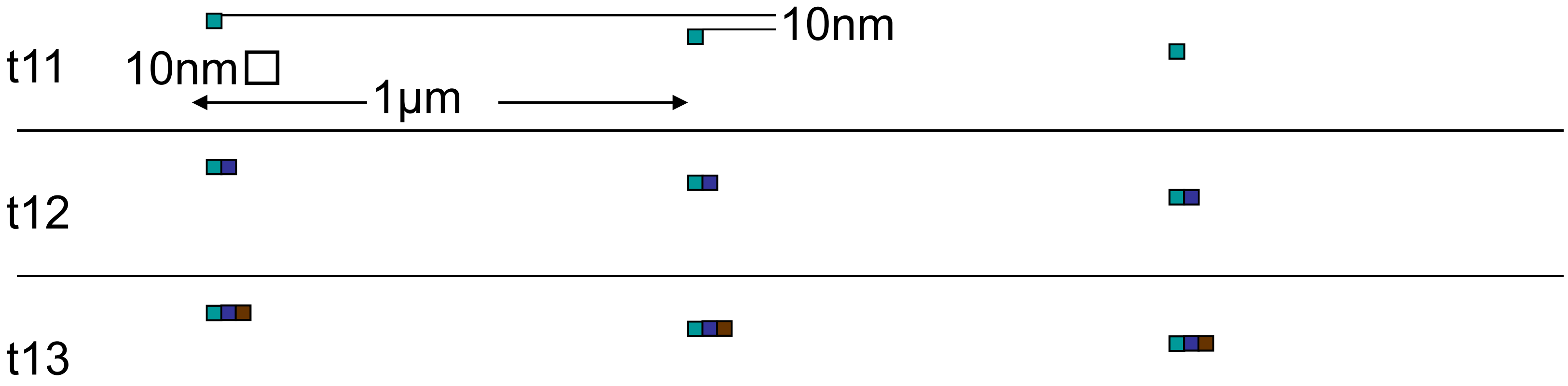


Design of micro column (Crestec, Kojima)

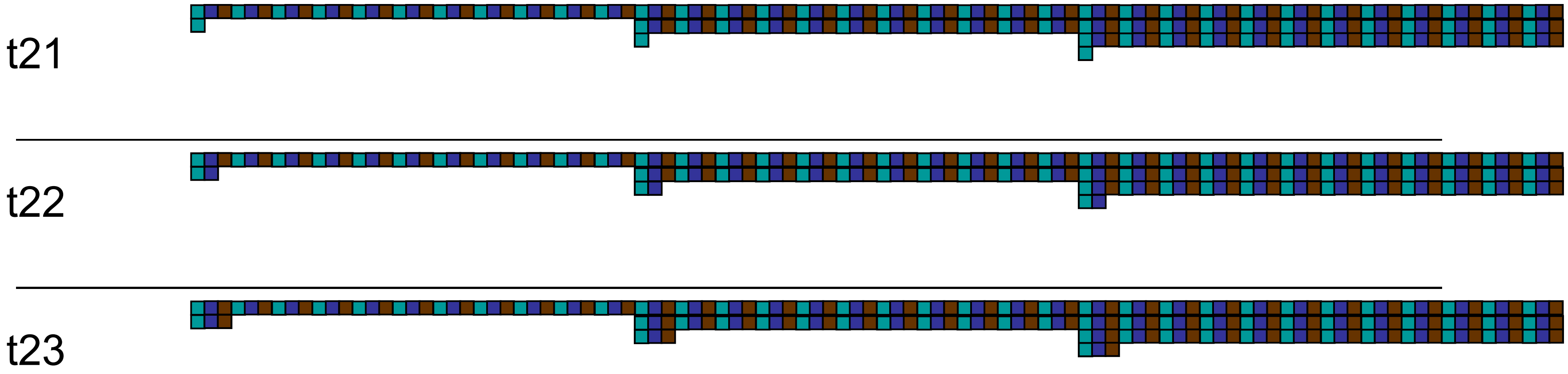
Active matrix nano-crystalline Si electron emitter



Fabrication of precise electrostatic lens

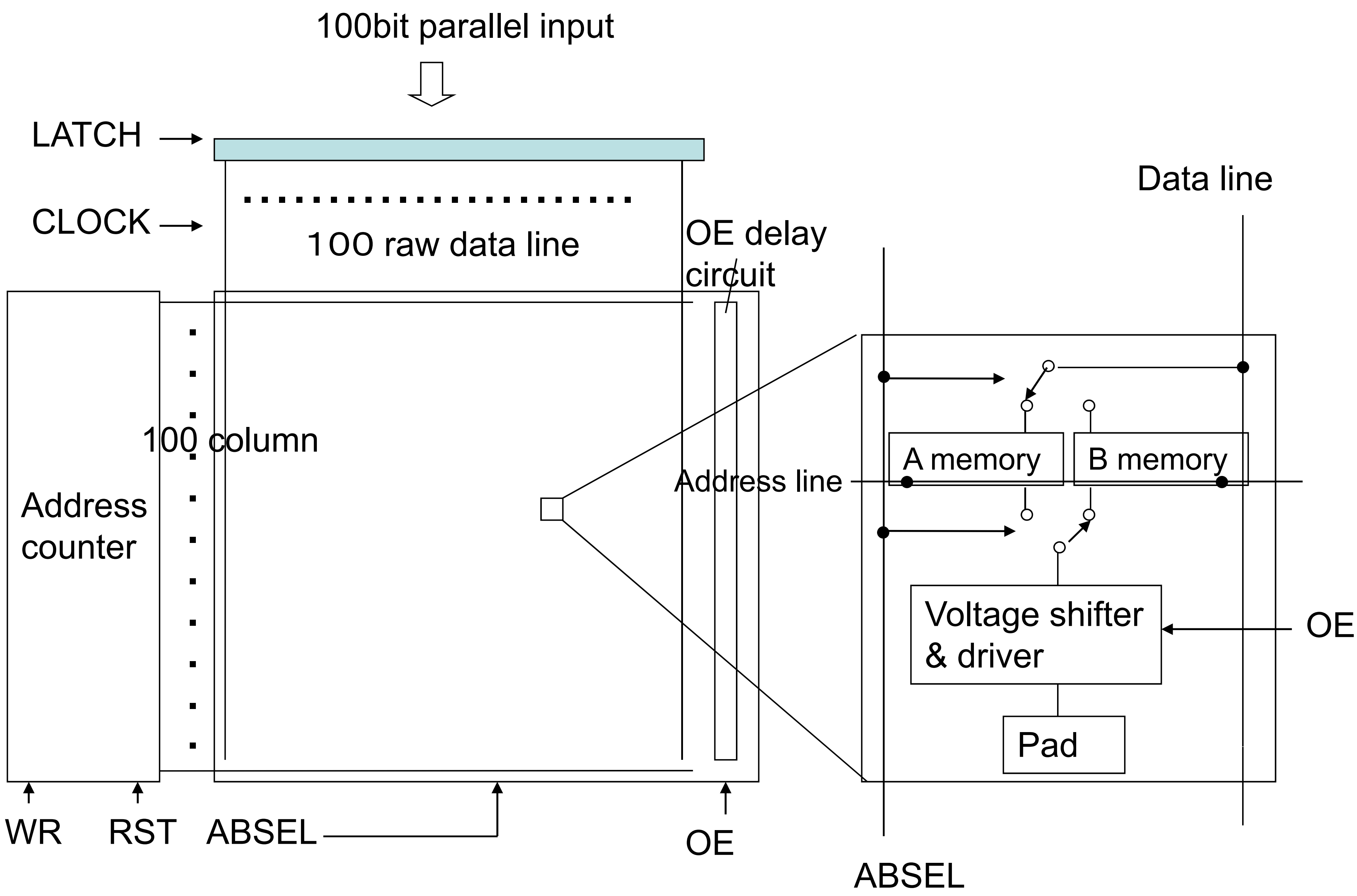


Exposure of the 1st line

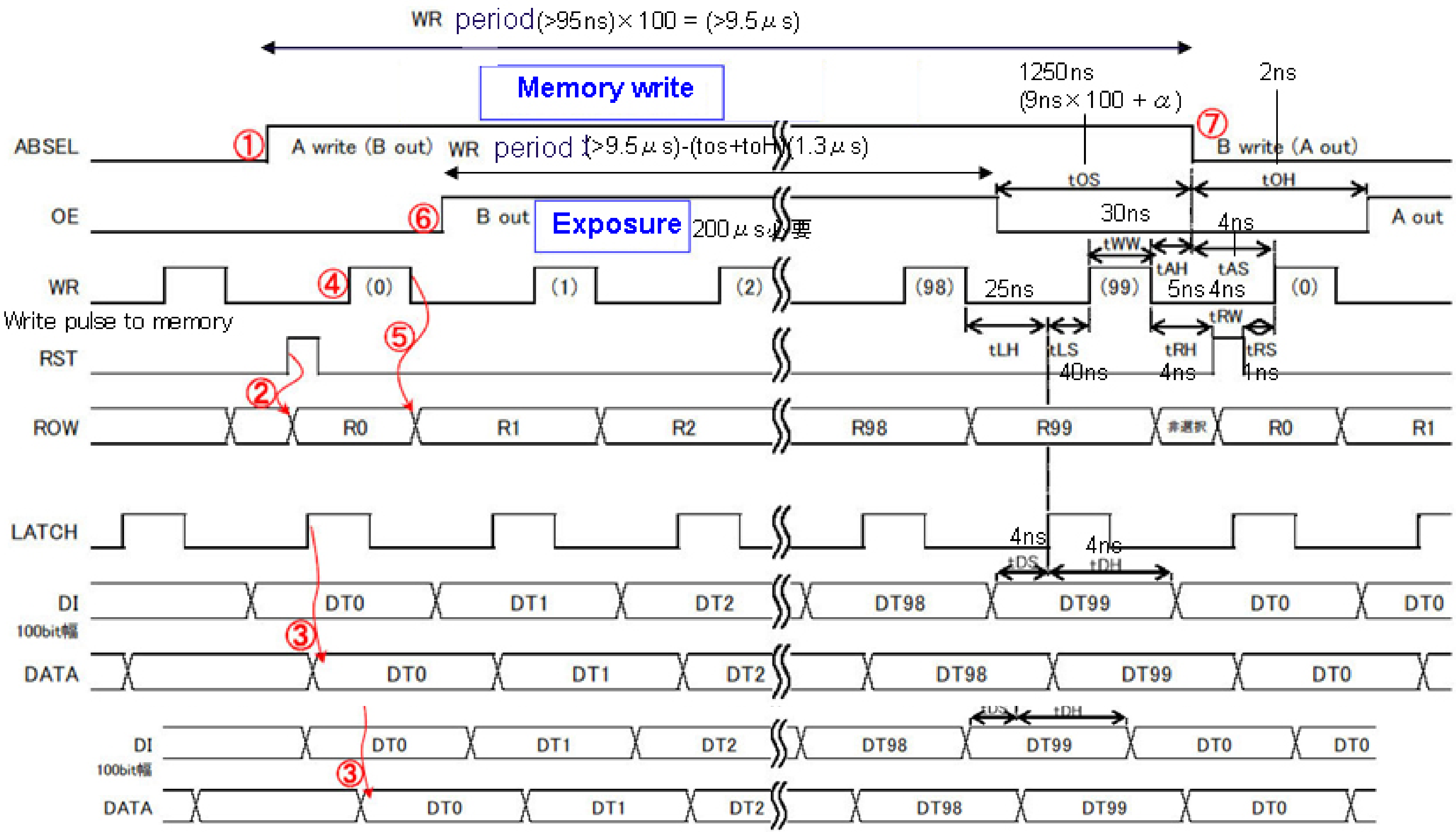


Exposure of the 2nd line

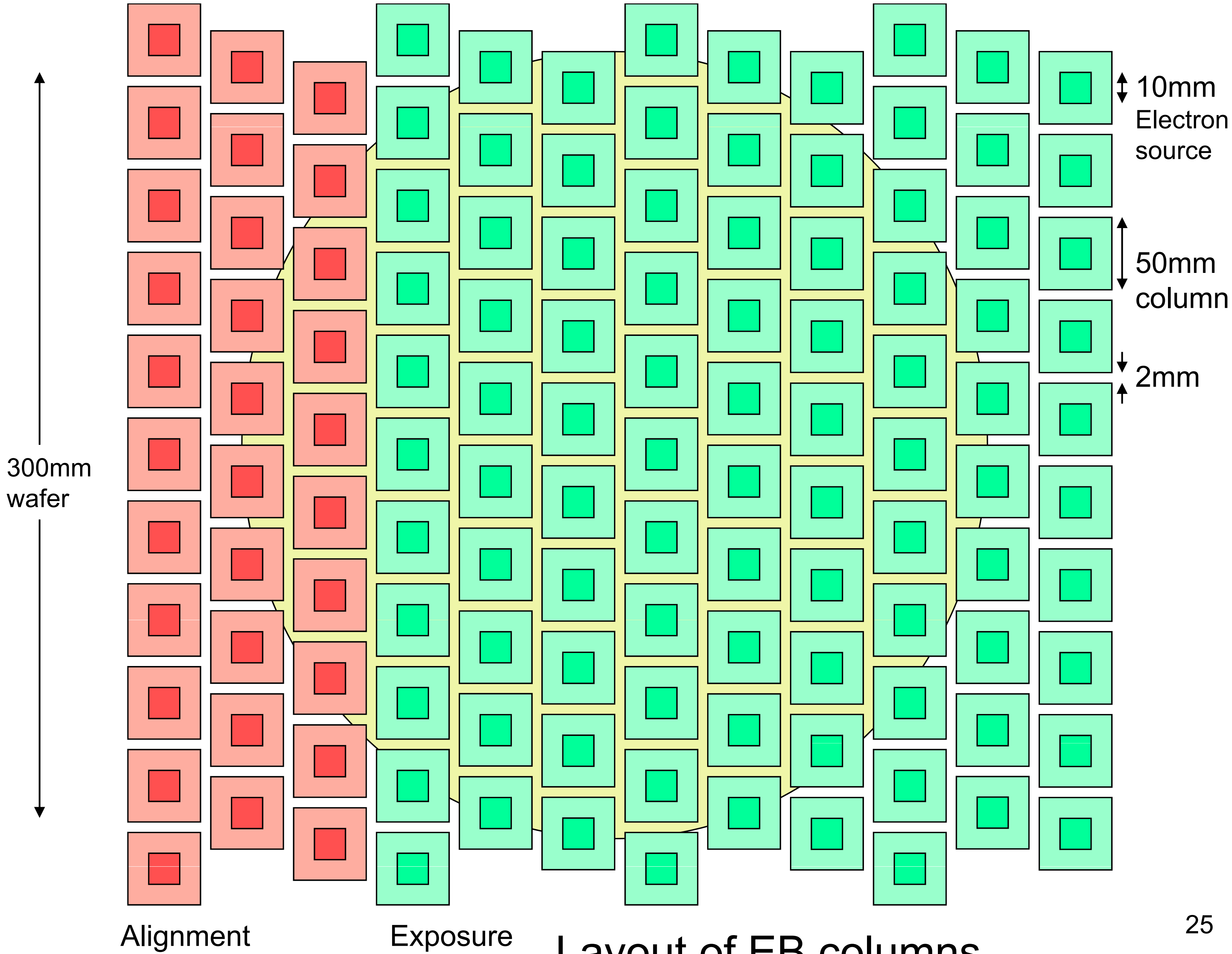
Exposure on wafer by one column



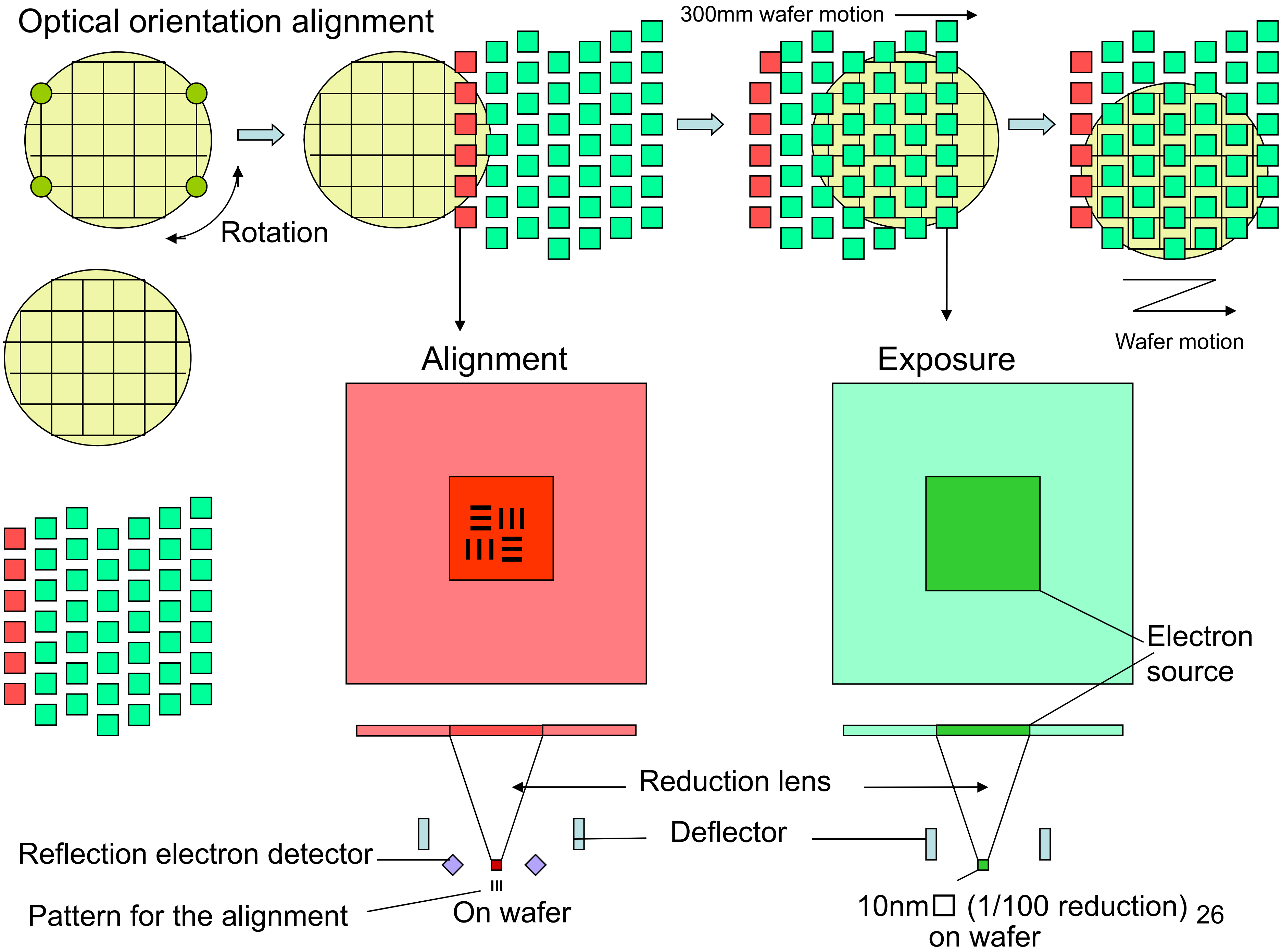
Active matrix circuits for the nanocrystal Si emitter



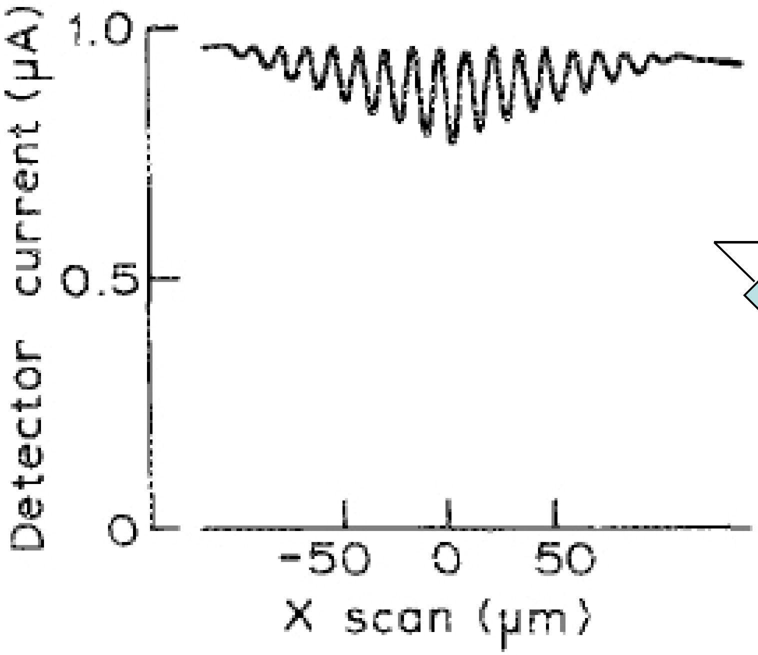
Timing chart

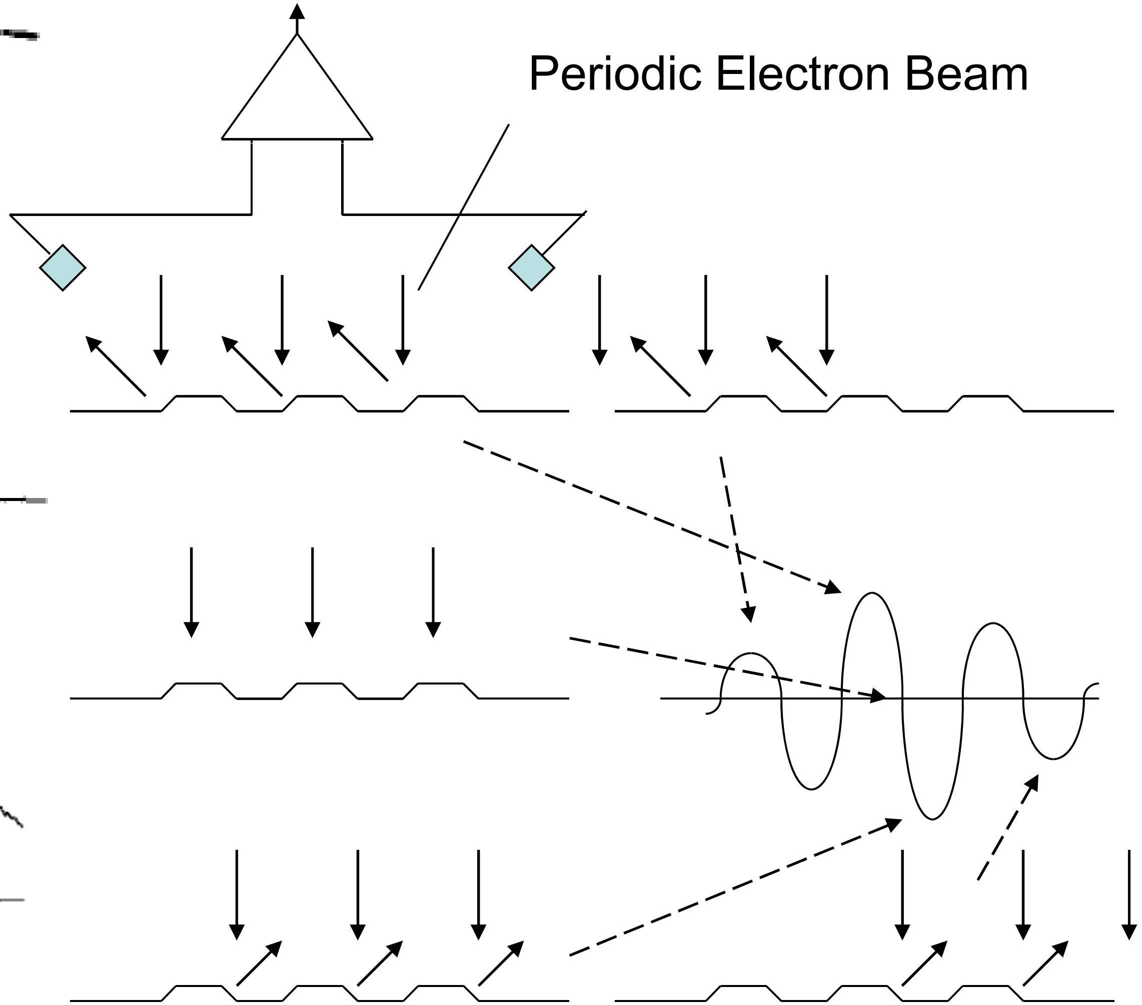


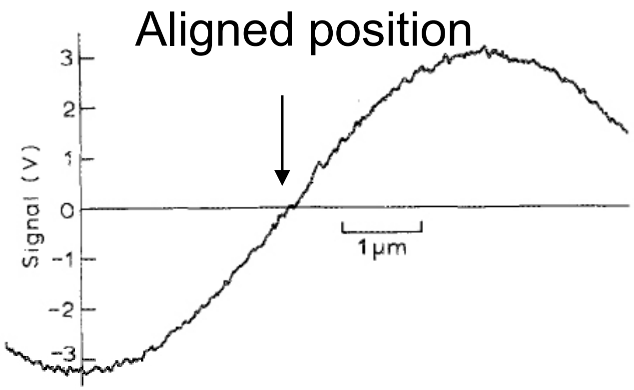
Layout of EB columns



Optical orientation alignment
Rotation
300mm wafer motion
Wafer motion
Alignment
Exposure
Electron source
Reduction lens
Deflector
Reflection electron detector
Pattern for the alignment
On wafer
10nm□ (1/100 reduction) on wafer



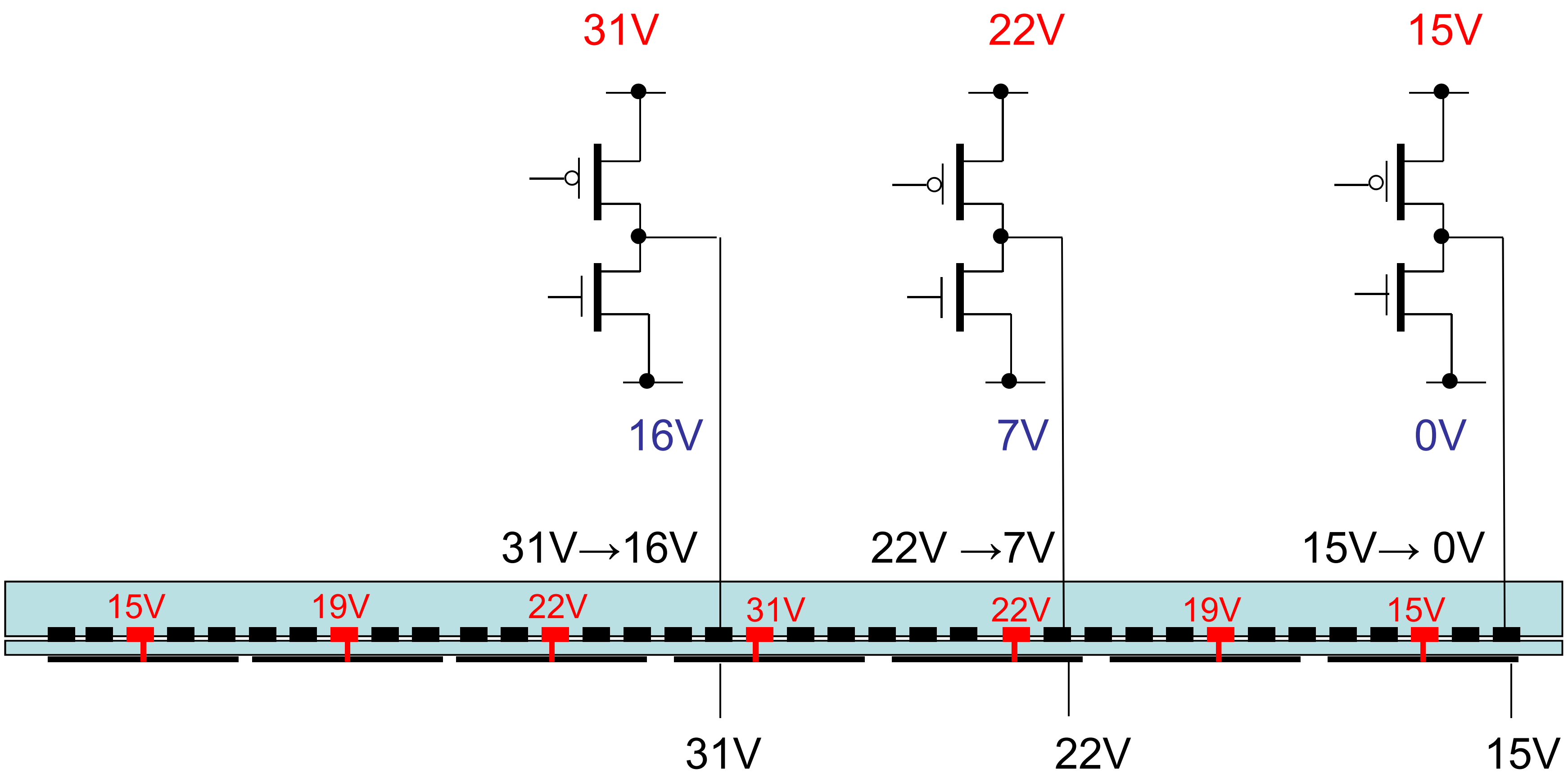




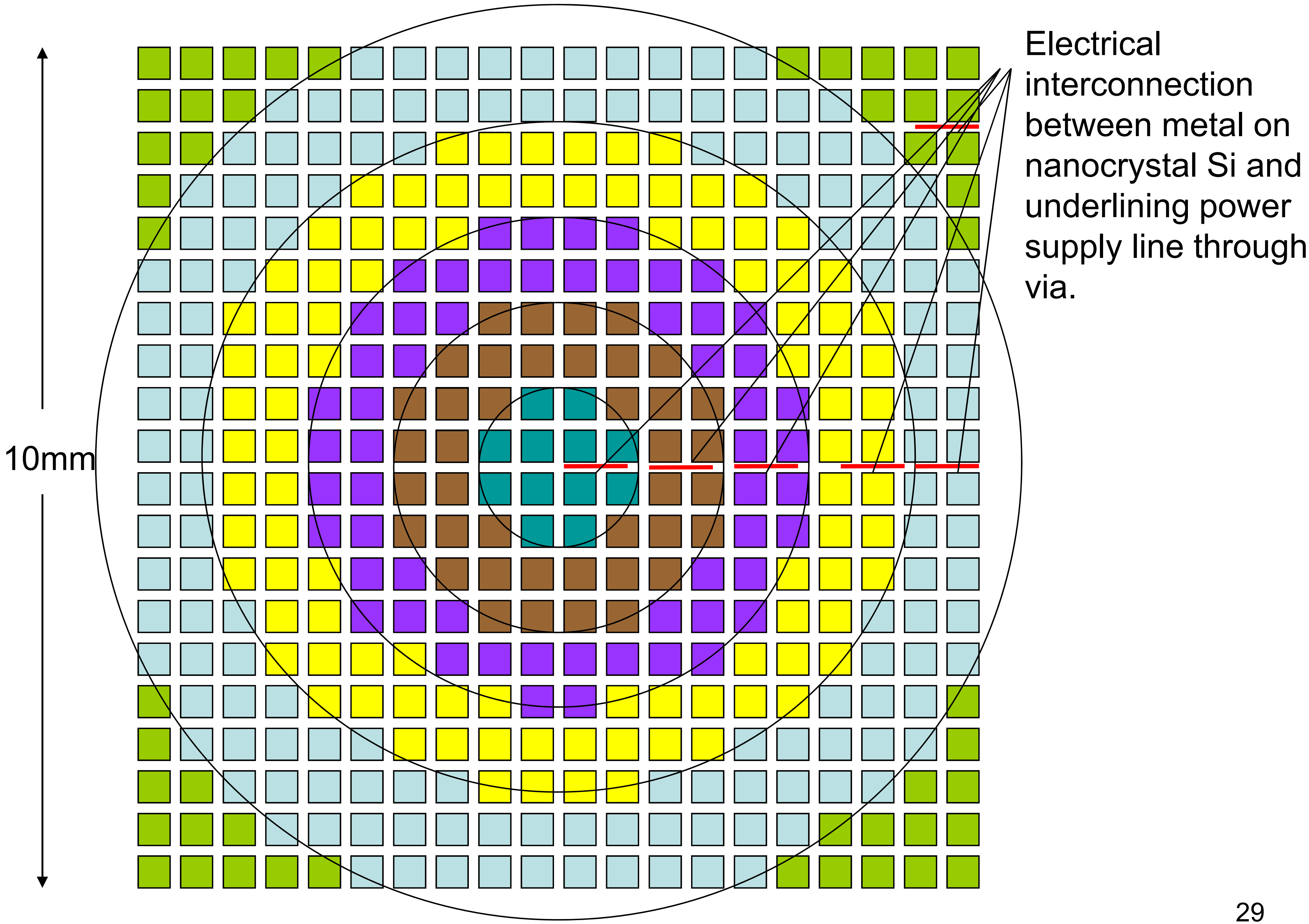
After phase sensitive detection

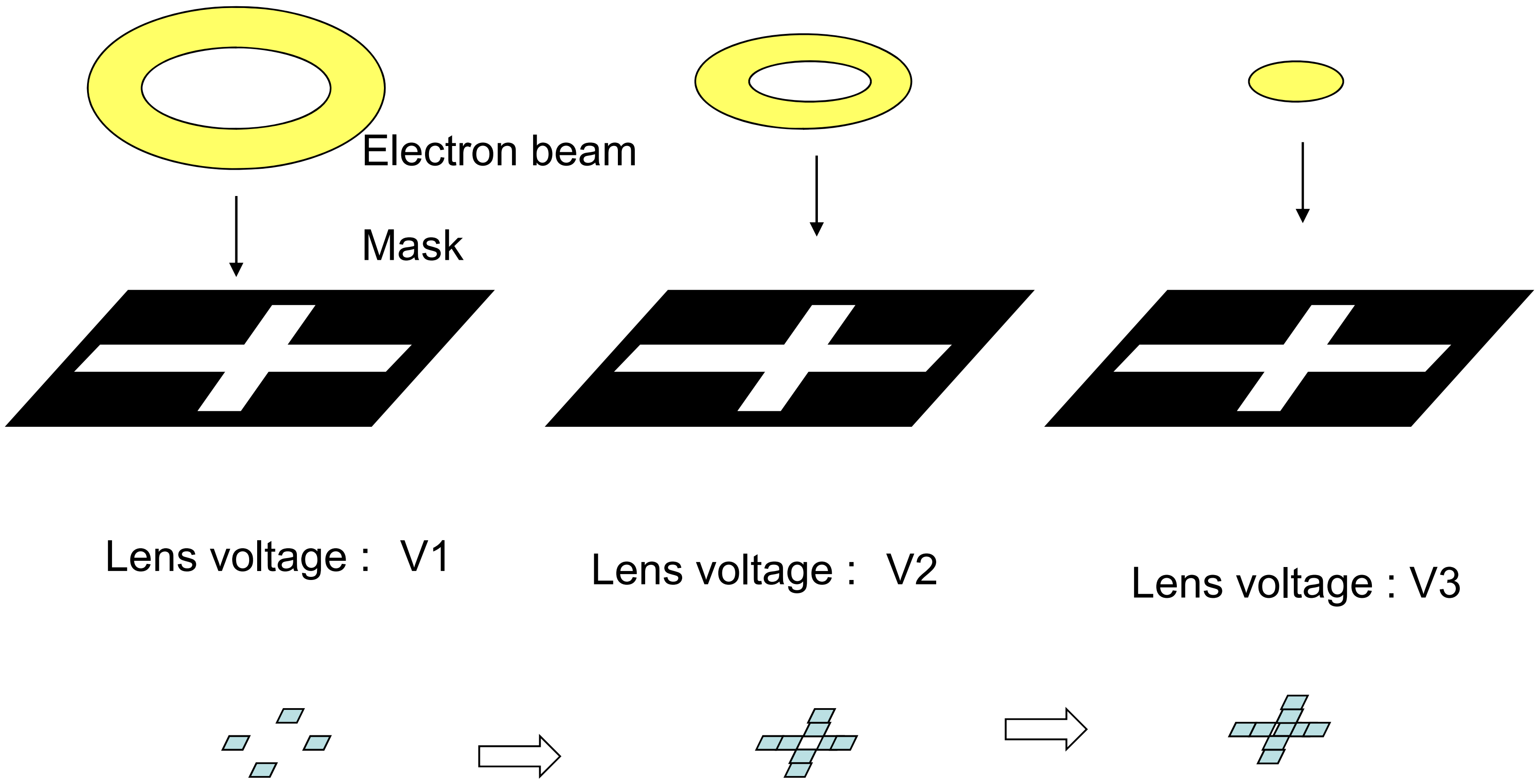
Principle of EB alignment

(R.Ward (Philips), J.Vac. Sci. Tec. B, 4 (1986) 89)



Driving voltages to the emitters are varied for focusing depending on the position on the chip


10mm
Electrical interconnection between metal on nanocrystal Si and underlining power supply line through via.



CVAL (Curvilinear Variable Axis Lens) used for focusing in PREVAIL (Projection Exposure with Variable Axis Immersion Lenses) system in IBM

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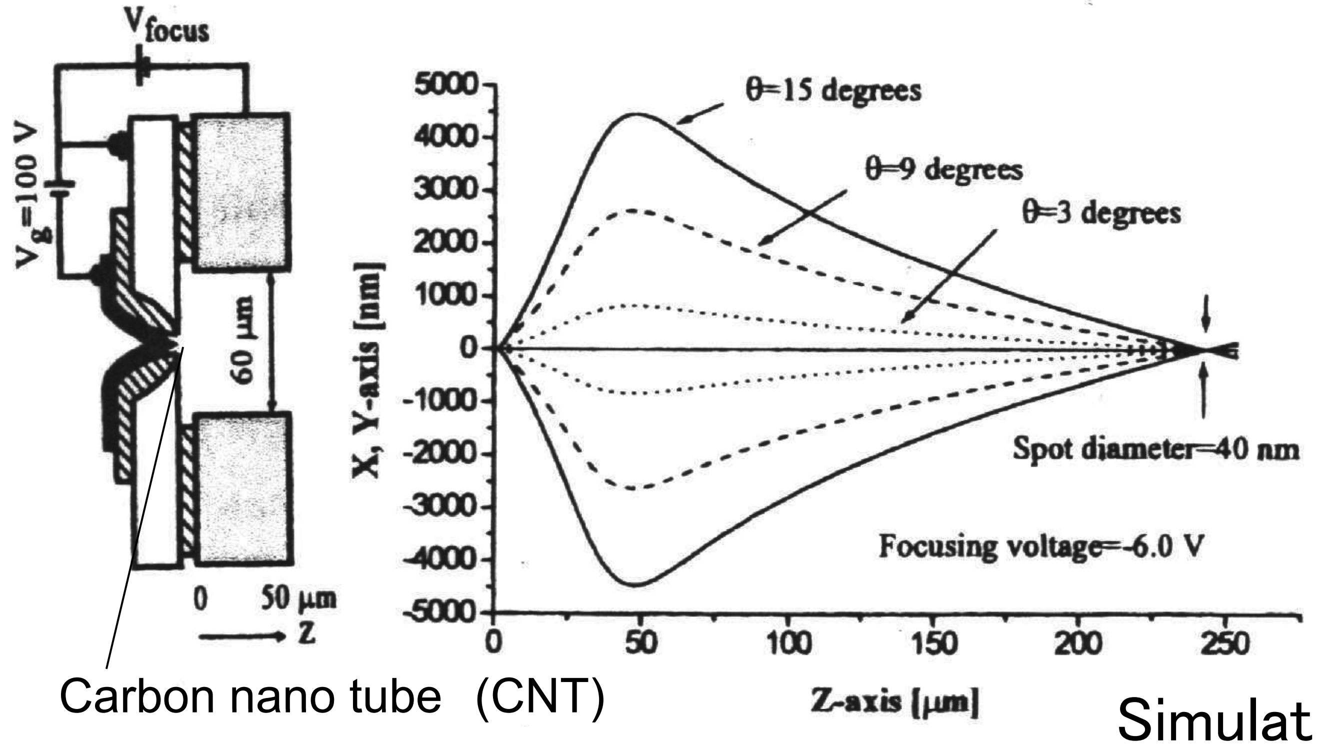
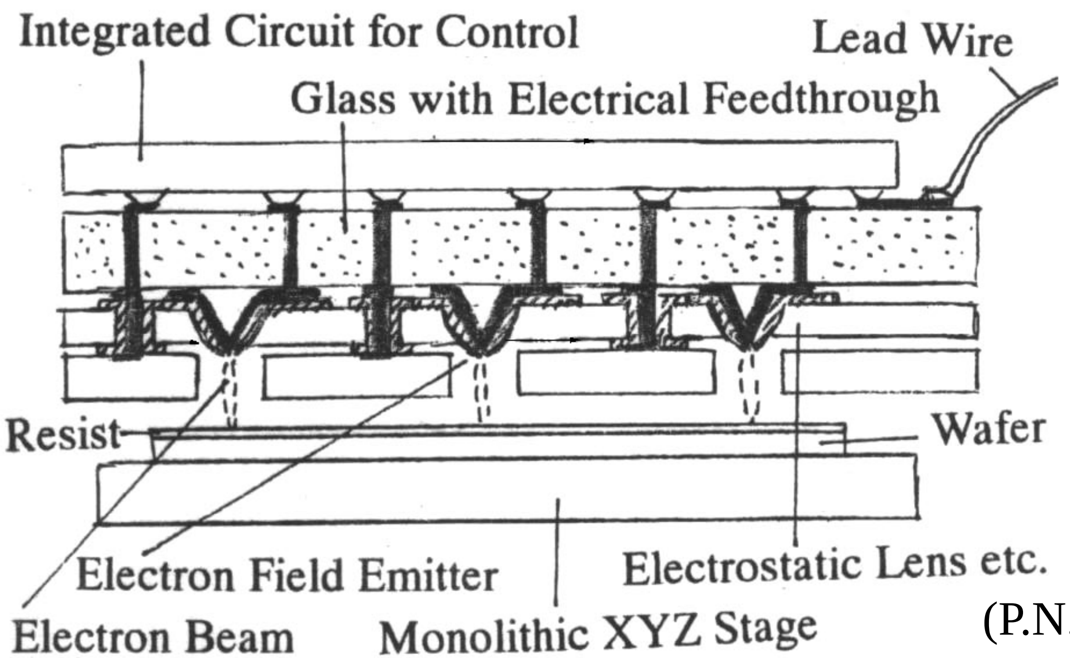
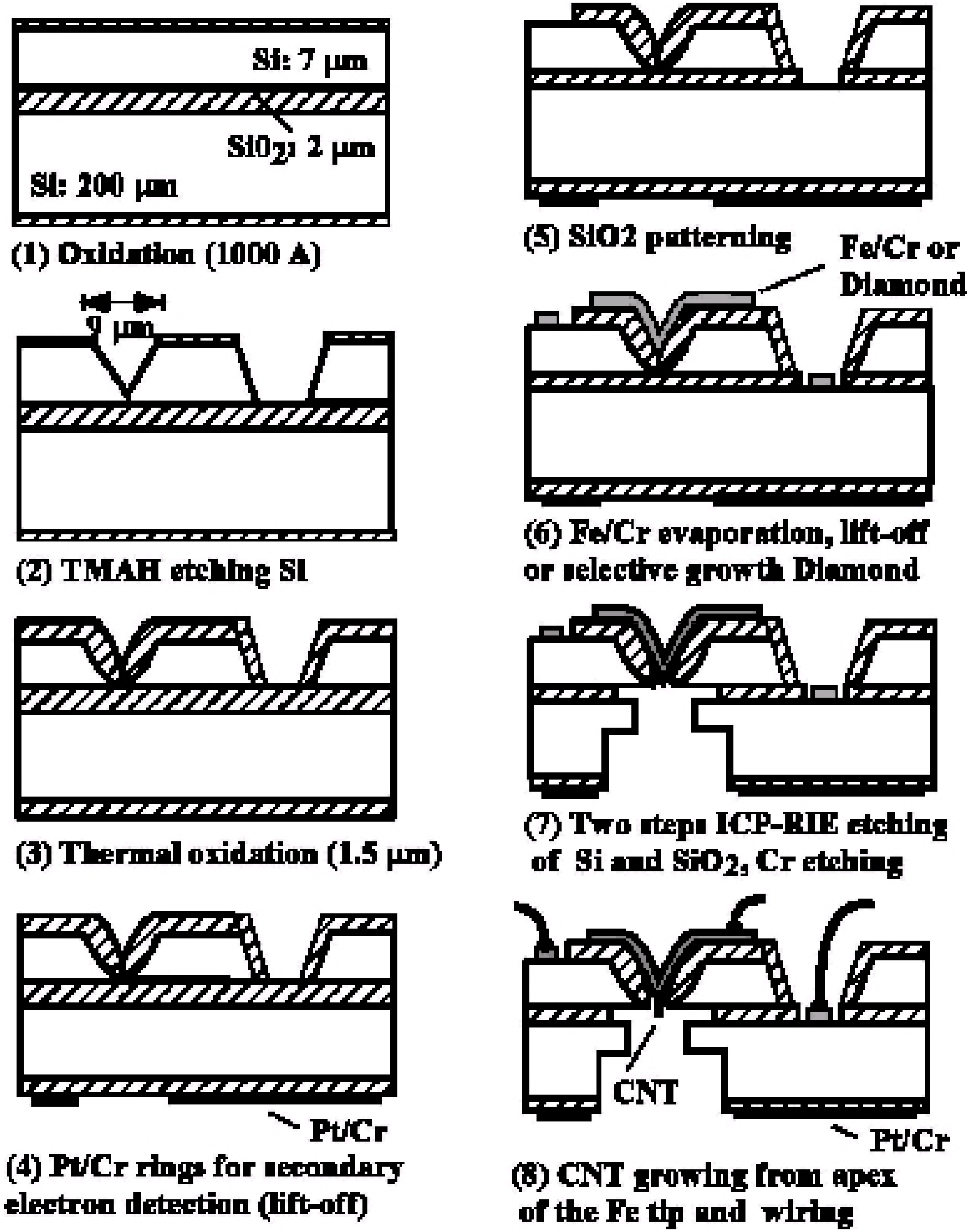


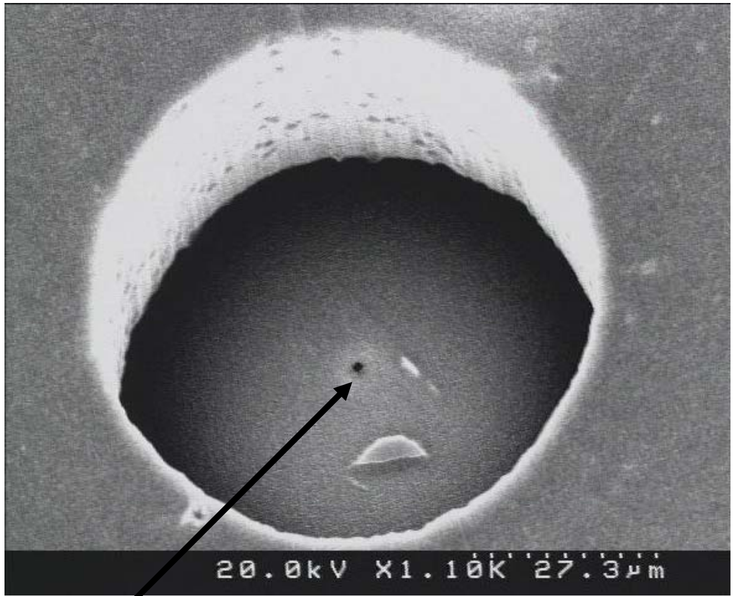
Simulation of electron beam focusing using carbon nano tube (CNT) emitter



Massive Parallel Electron Beam Lithography

(P.N.Minh, MEMS'04 (2004), p.430)



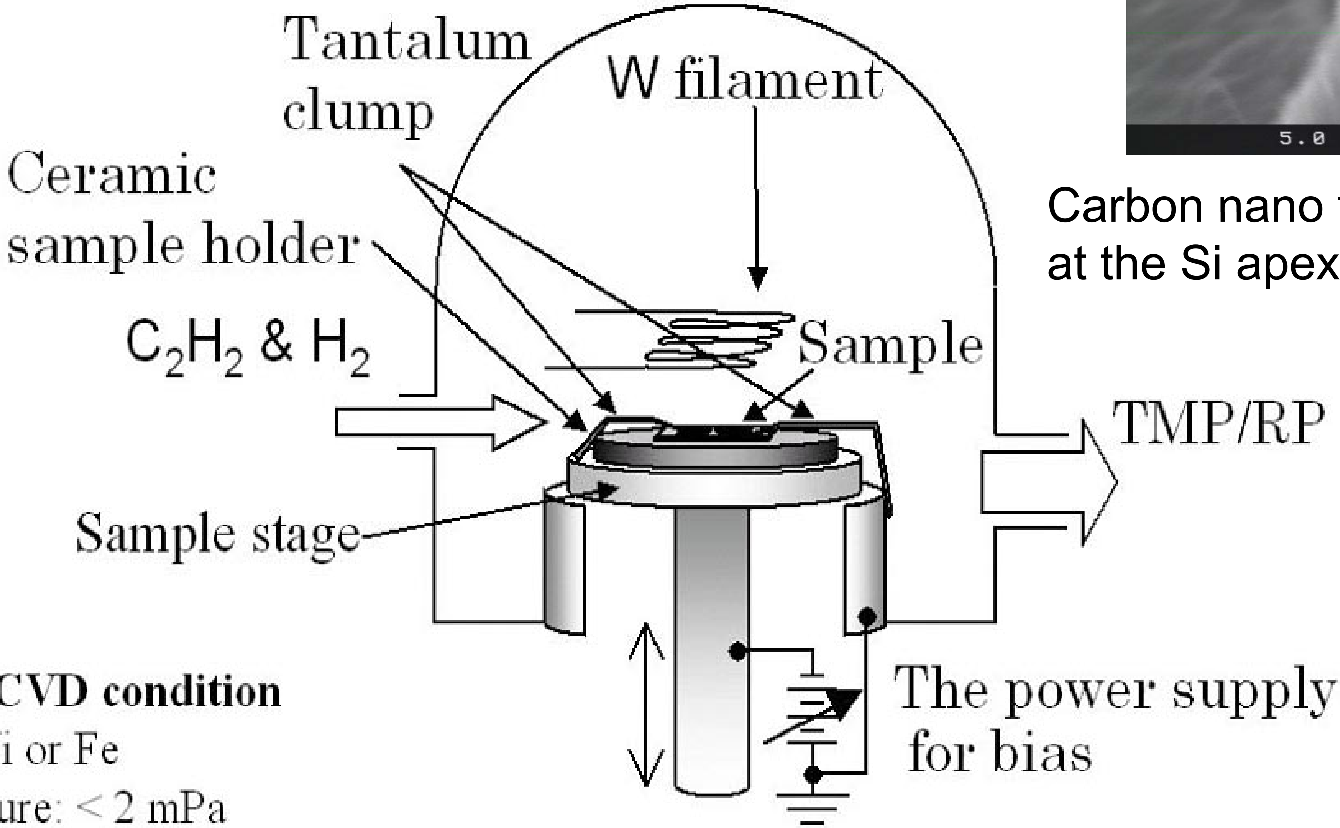


CNT electron field emitter

Fabrication of electron field emitter array with electrostatic lens

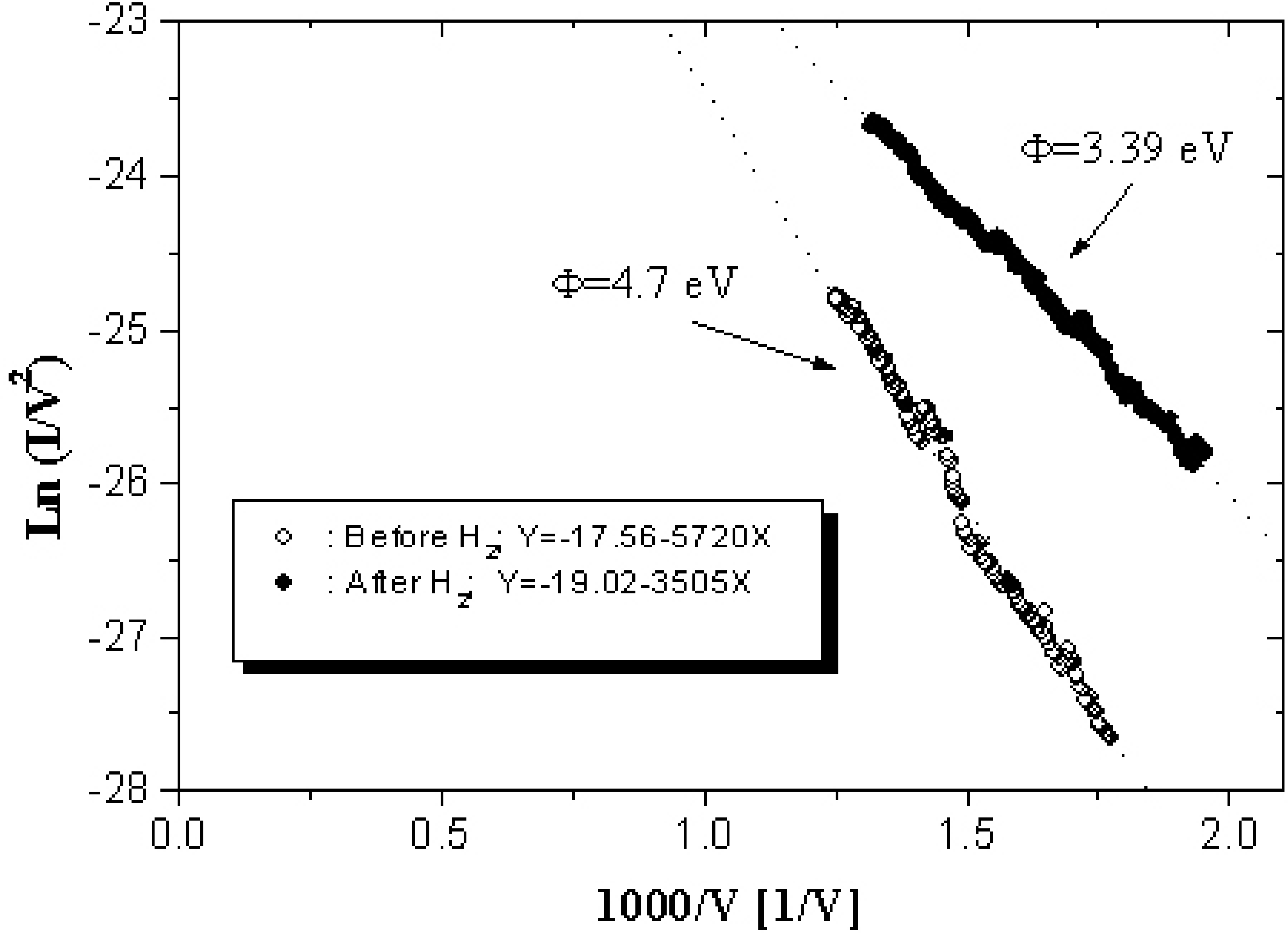
(P.N.Minh, MEMS'04 (2004), p.430)

Carbon nano tube deposited at the Si apex

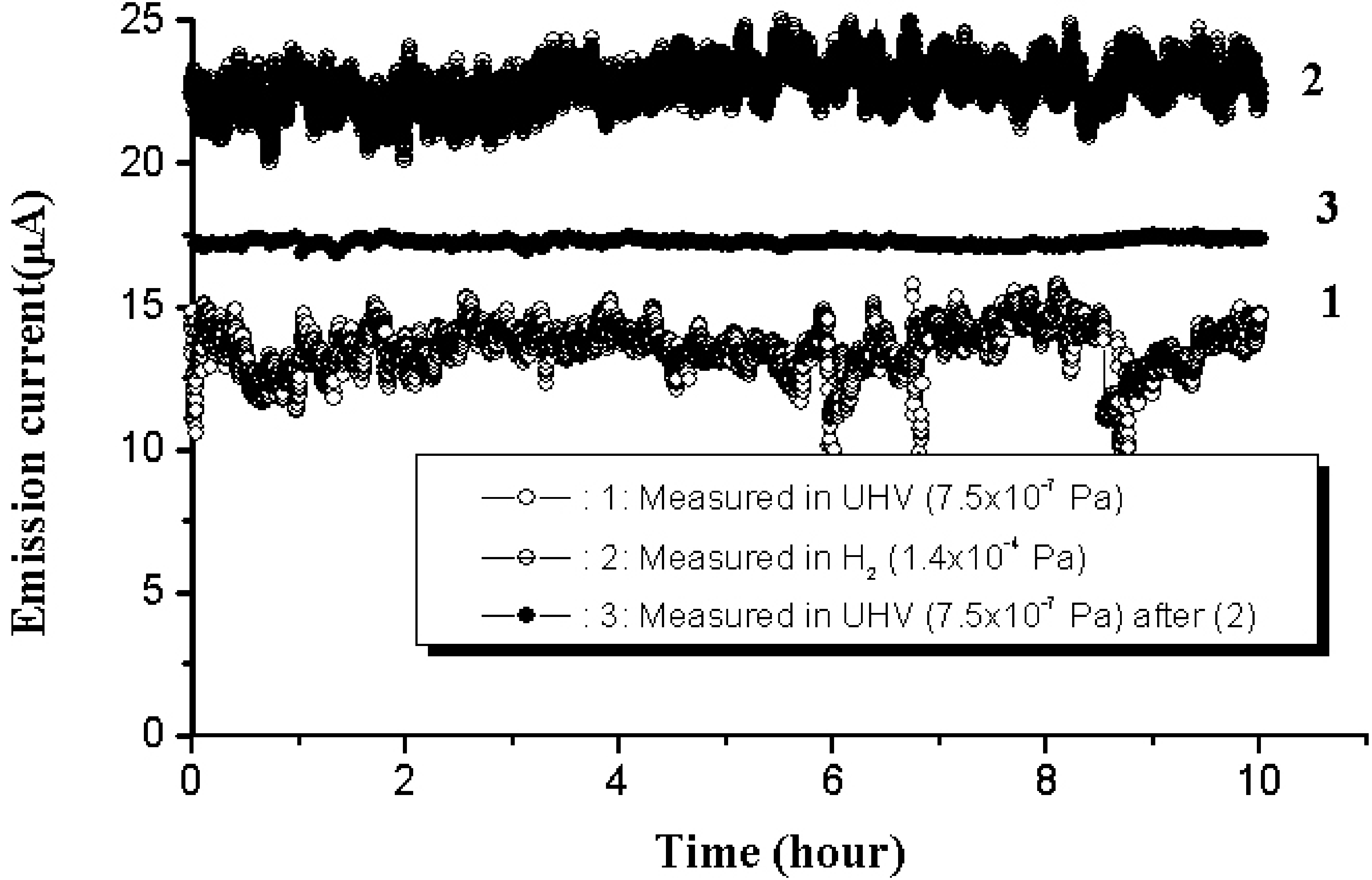


Normally CVD condition
Catalyst: Ni or Fe
Back pressure: < 2 mPa
Gas: C_2H_2 3 Pa, H_2 27 Pa
Distance from filament to sample: 5 mm
Filament temp.: 1900 °C
Sample temp: about 600 °C

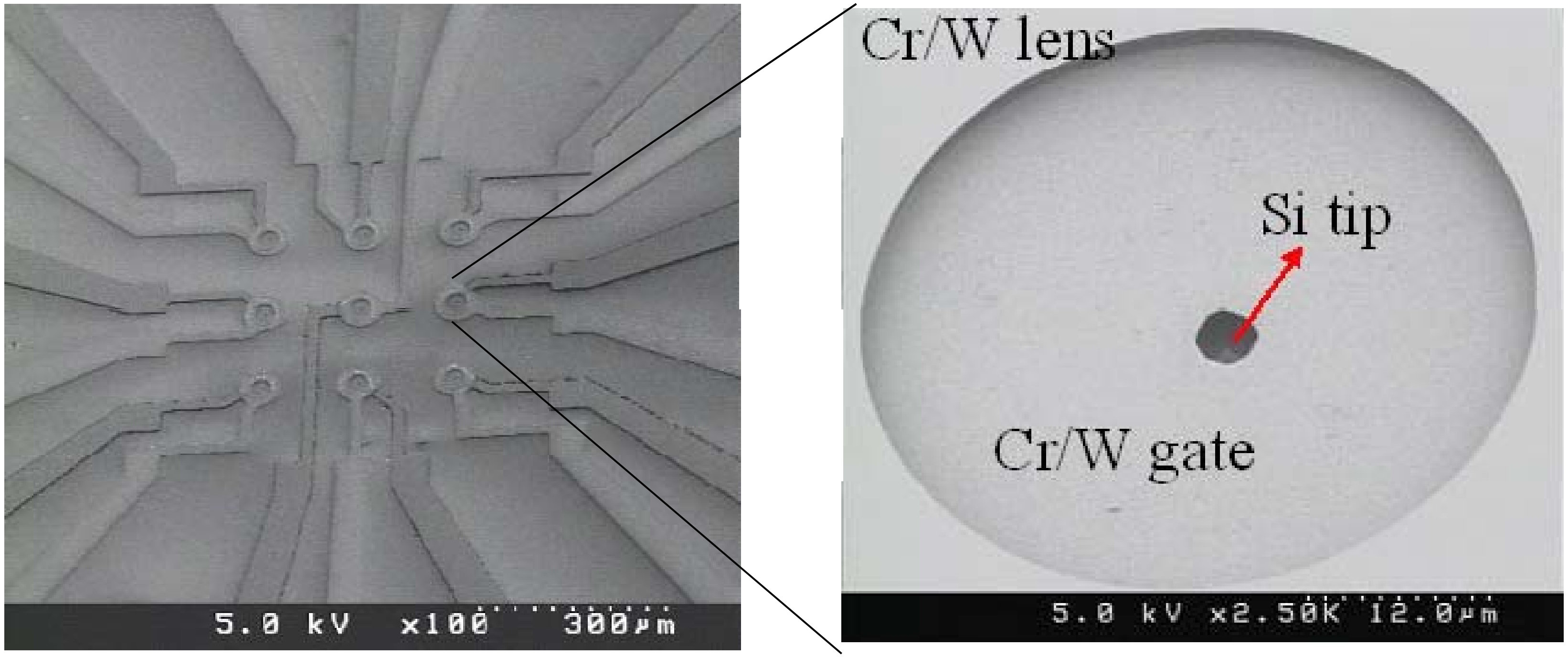
Hot filament CVD of carbon nano tube
(H.Miyashita et.al. MEMS'2001)

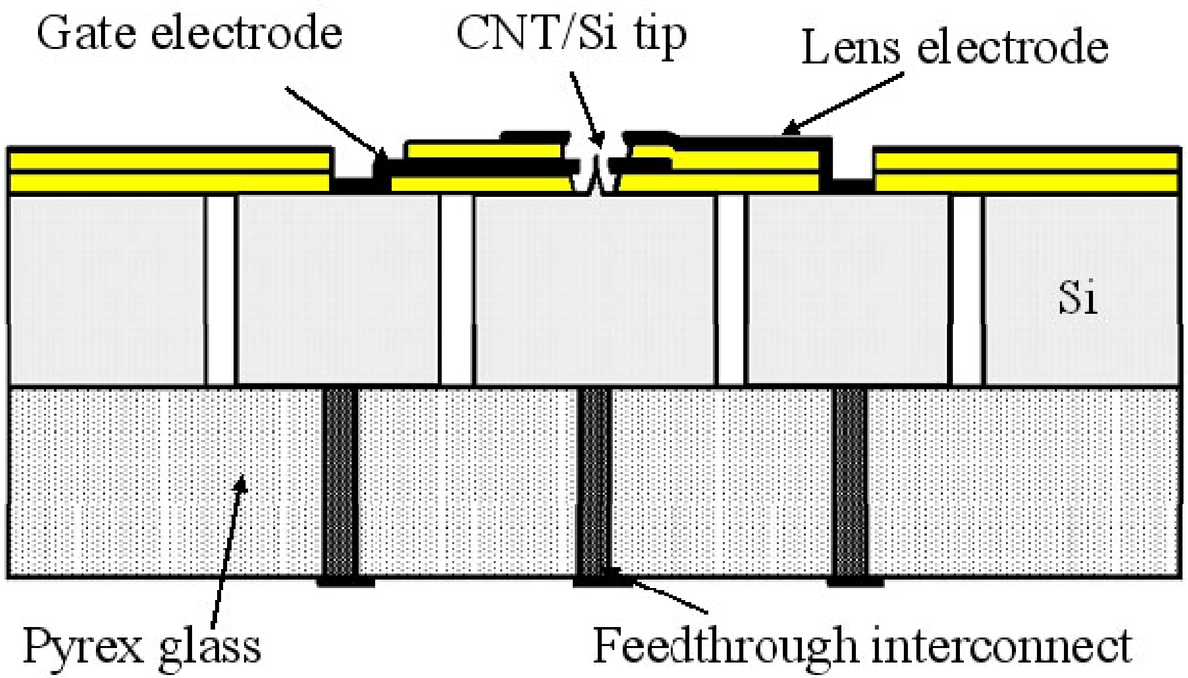


Effect of hydrogen treatment (Fowler-Nordheim plot) (P.N.Minh, MEMS'04 (2004), p.430)

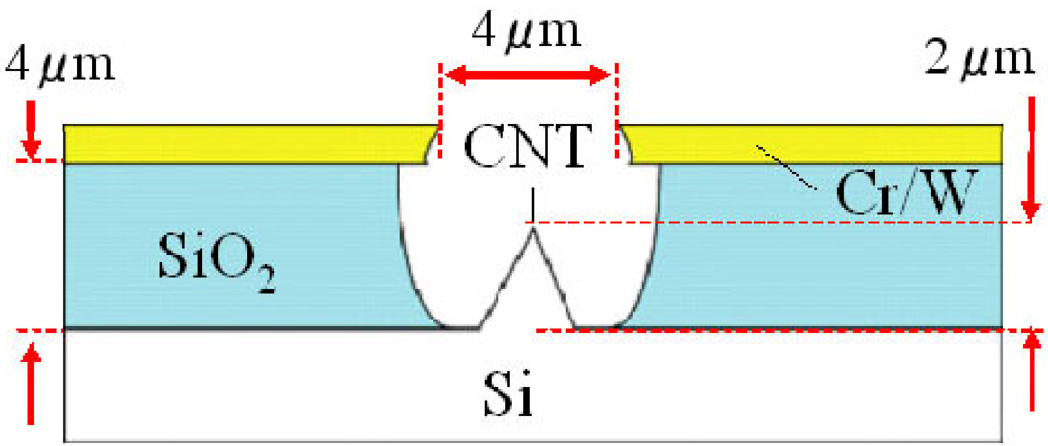


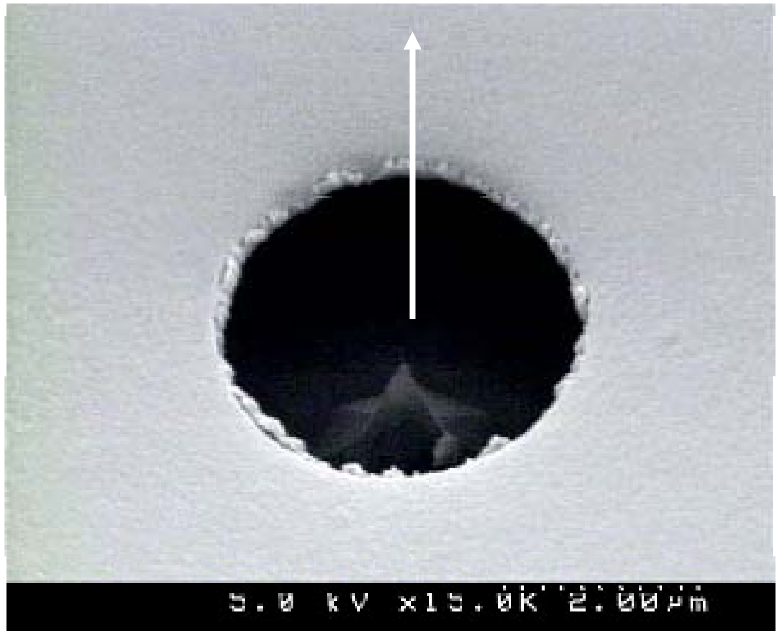
Stability of carbon nanotube field emitter

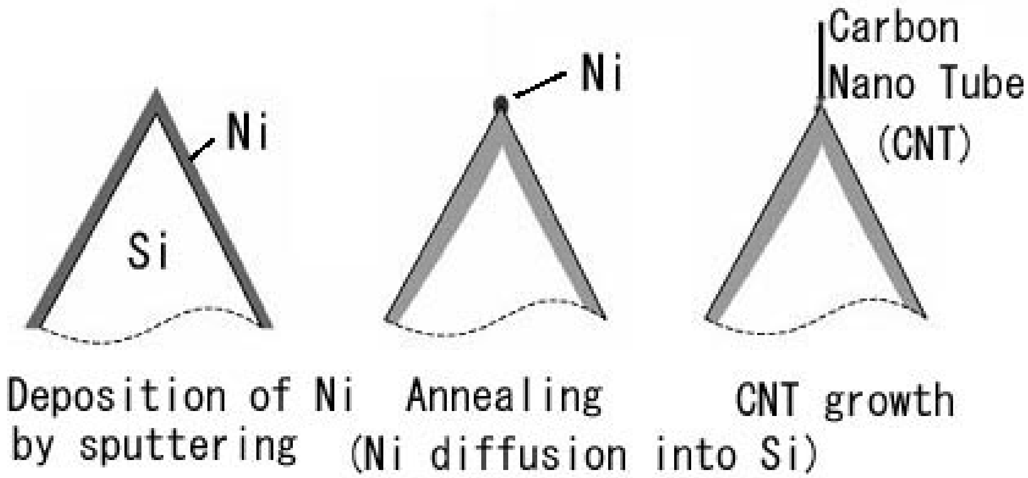




3 x 3 electrostatic lens integrated field emission array

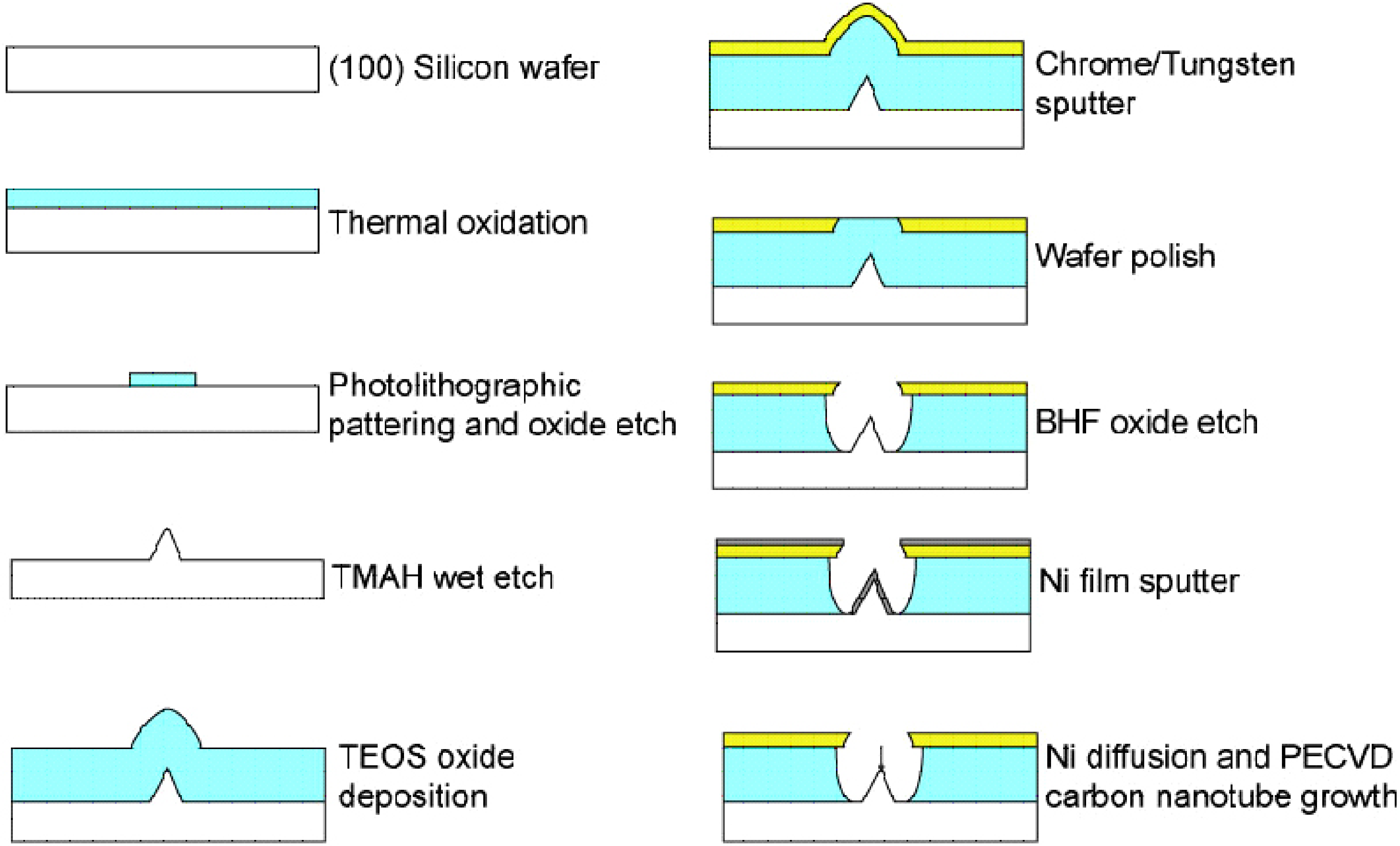




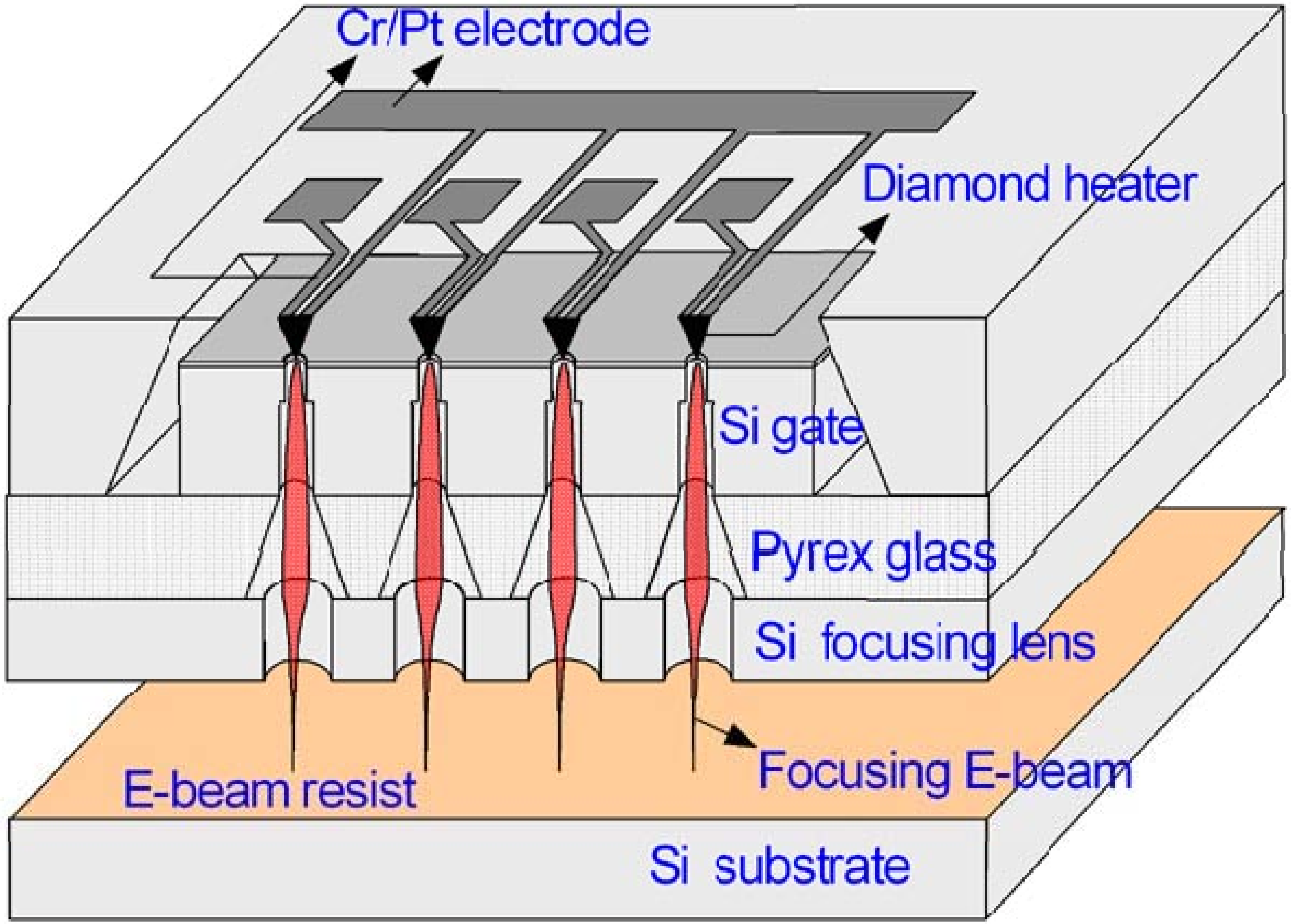


Carbon nano tube emitter with gate

(J.Y.Ho, T.Ono & M.Esashi, 33th Intnl. Conf. on Micro- and Nano-Engng., Copenhagen (Denmark), (2007/9/23-26))

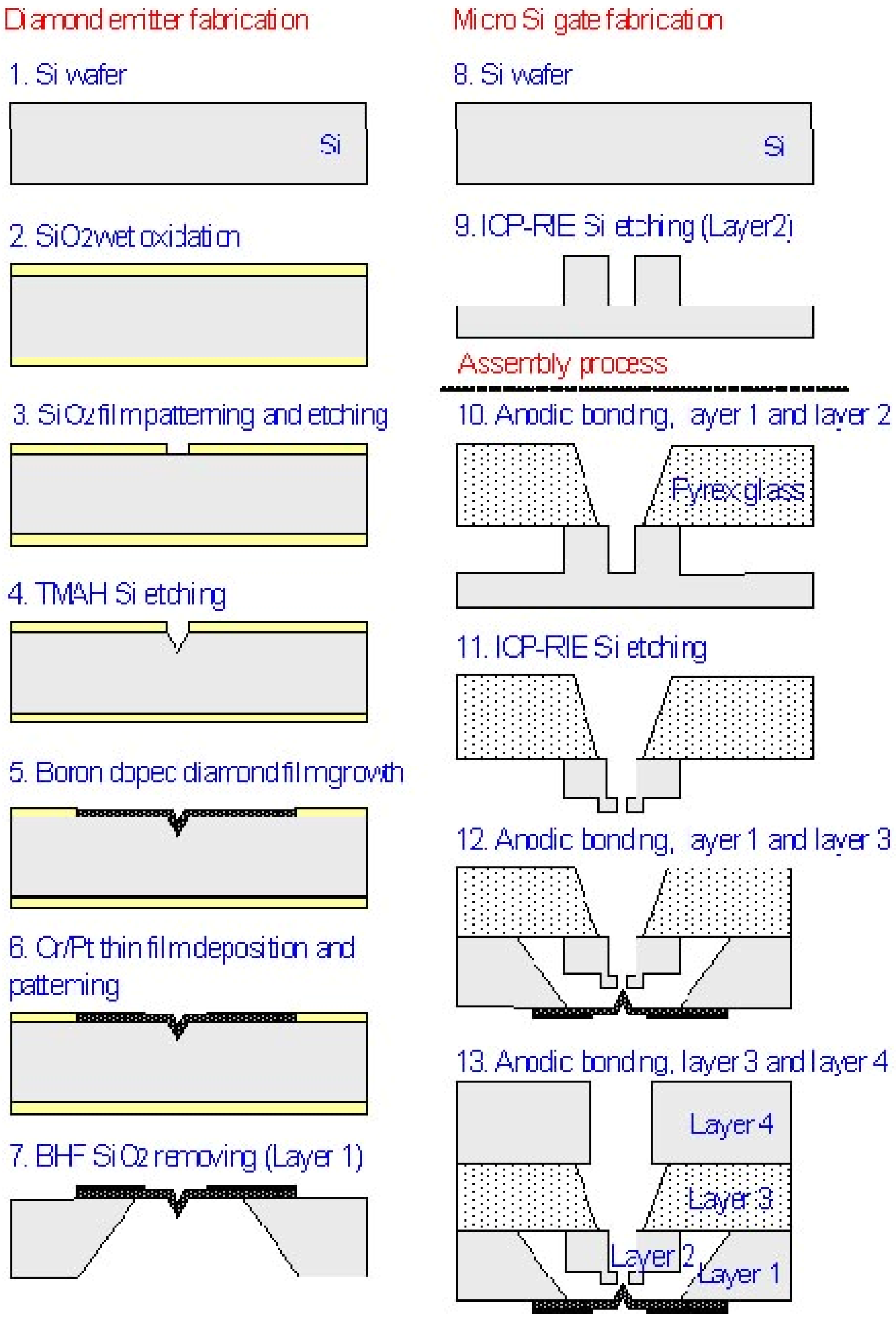


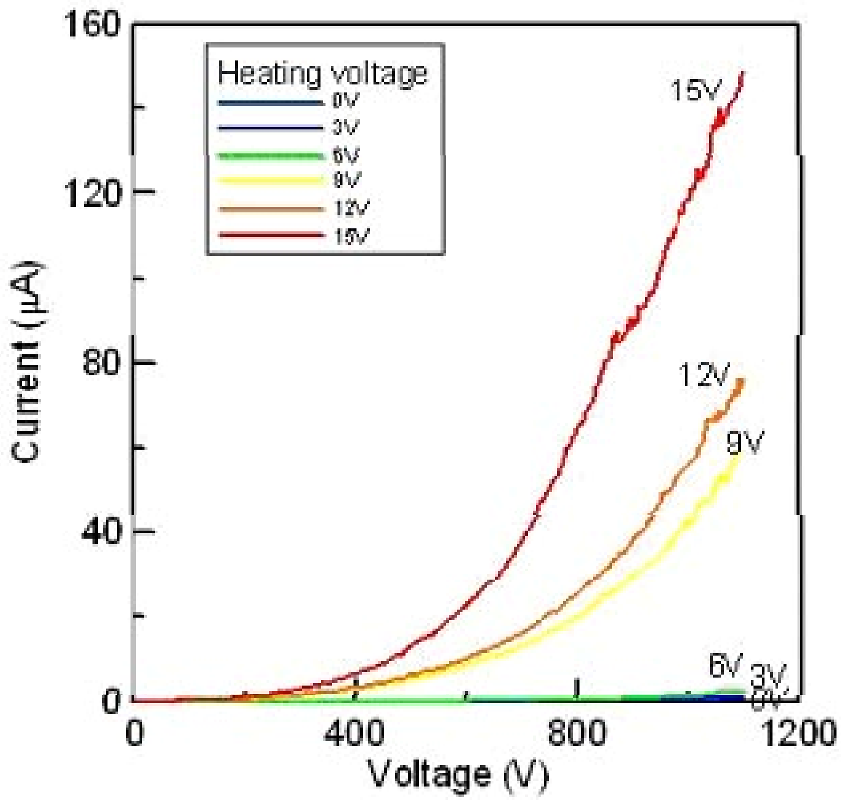
Fabrication process of carbon nanotube emitter with gate
(J.Y.Ho, T.Ono & M.Esashi, 33th Intnl. Conf. on Micro- and Nano-Engng., Copenhagen (Denmark), (2007/9/23-26))

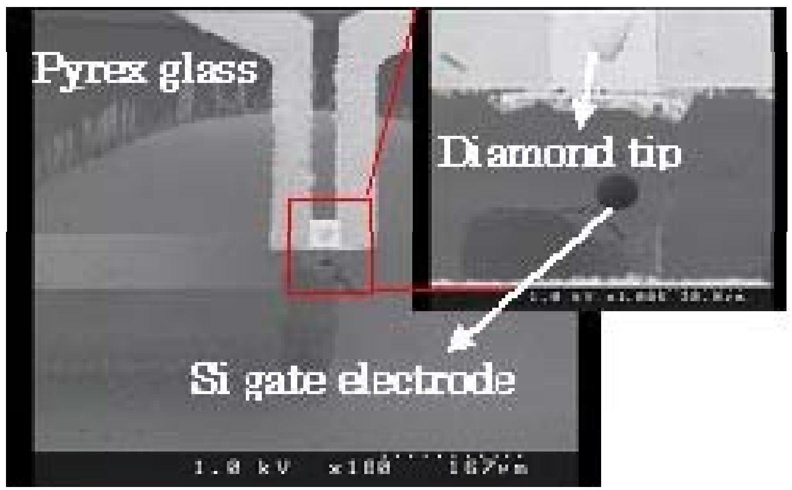


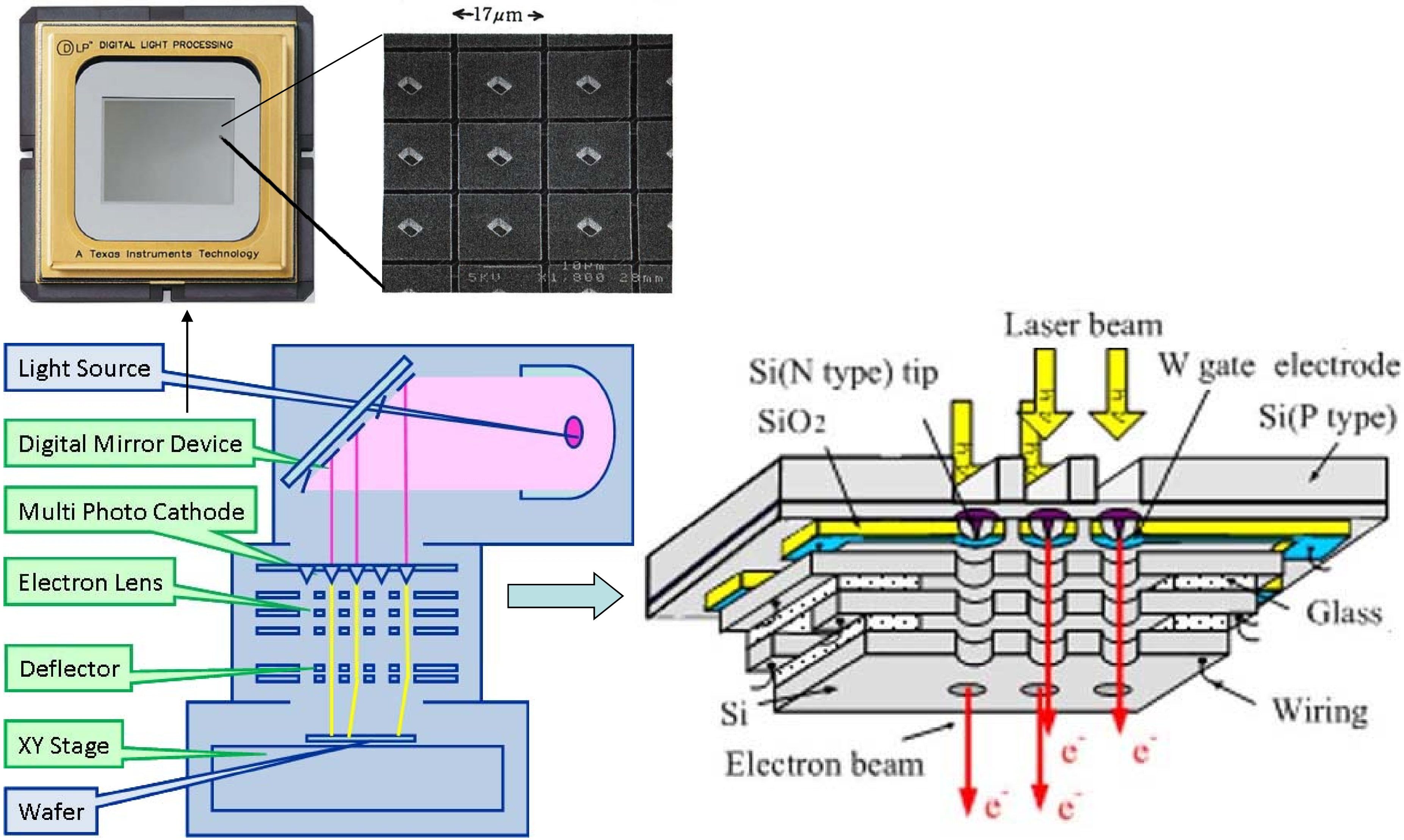
Diamond Shottky Emitter Array

(C.H.Tsai, APCOT 2006)


Diamond emitter fabrication
1. Si wafer
Si
2. SiO2 wet oxidation
3. SiO2 film patterning and etching
4. TMAH Si etching
5. Boron doped diamond film growth
6. Cr/Pt thin film deposition and patterning
7. BHF SiO2 removing (Layer 1)
Micro Si gate fabrication
8. Si wafer
Si
9. ICP-RIE Si etching (Layer2)
Assembly process
10. Anodic bonding, layer 1 and layer 2
Pyrex glass
11. ICP-RIE Si etching
12. Anodic bonding, layer 1 and layer 3
13. Anodic bonding, layer 3 and layer 4
Layer 4
Layer 3
Layer 2
Layer 1

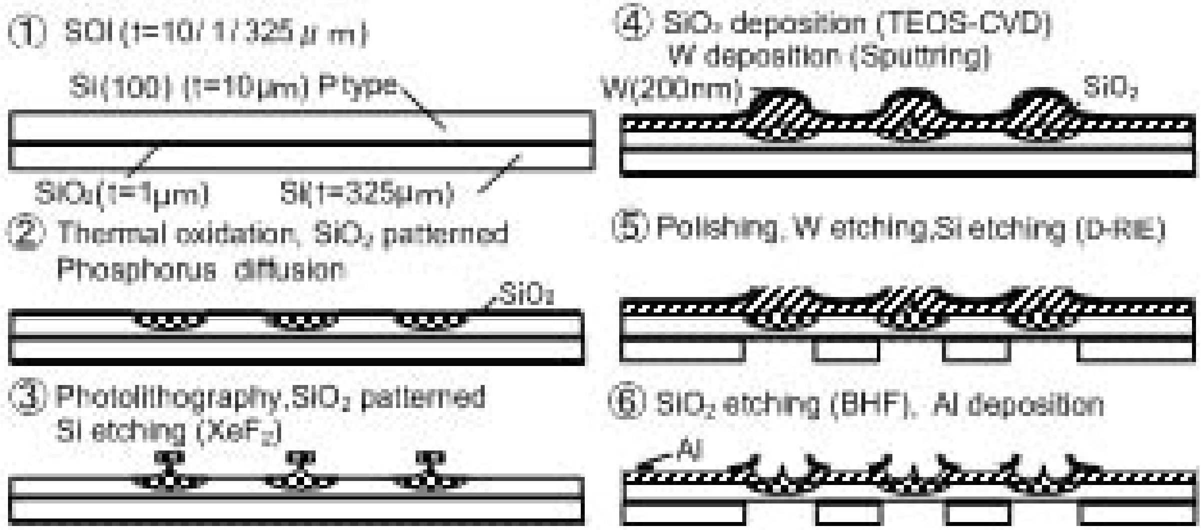

Heating voltage
0V
3V
6V
9V
12V
15V
Current (μA)
Voltage (V)
160
120
80
40
0
0
400
800
1200

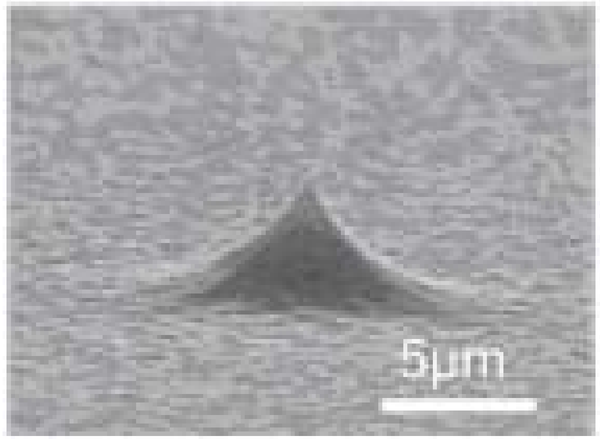

Pyrex glass
Diamond tip
Si gate electrode

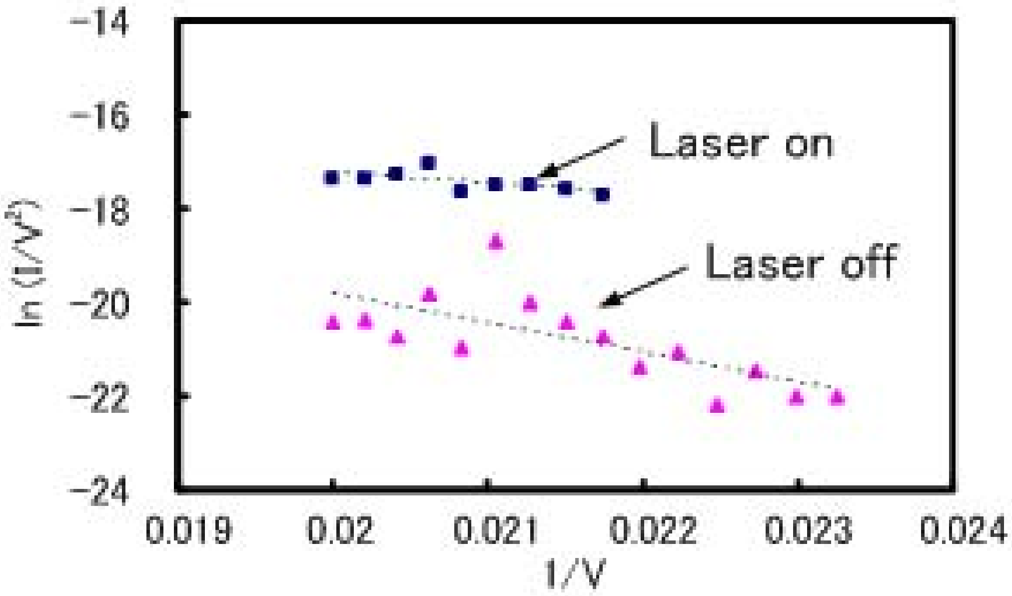


Photocathode multi-electron beam lithography

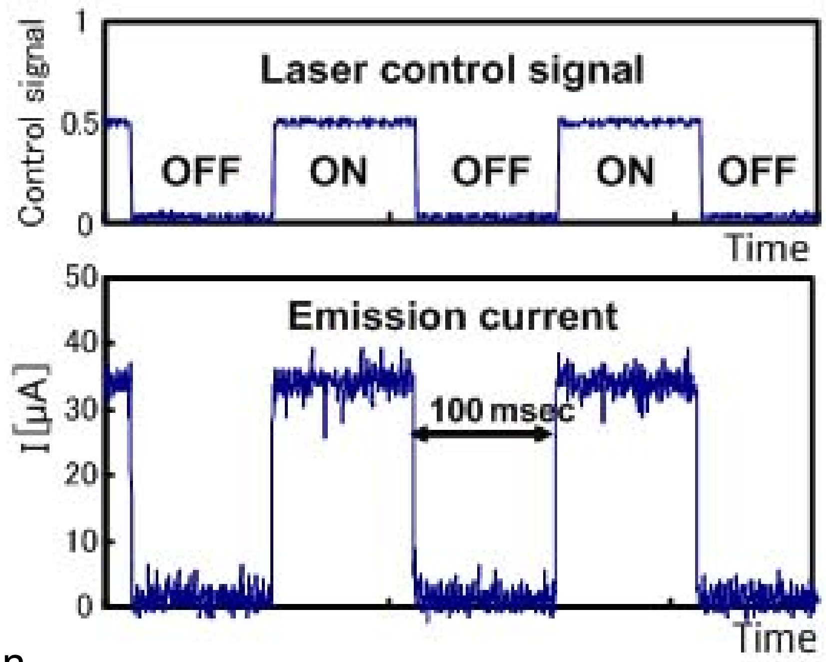
(E. Tomono, H. Miyashita, T. Ono and M. Esashi, APCOT 2010)



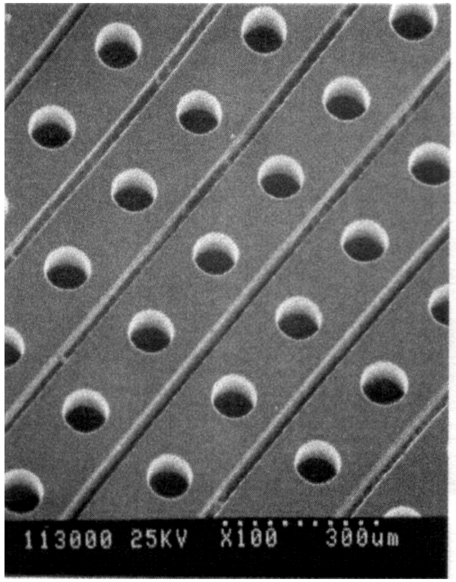


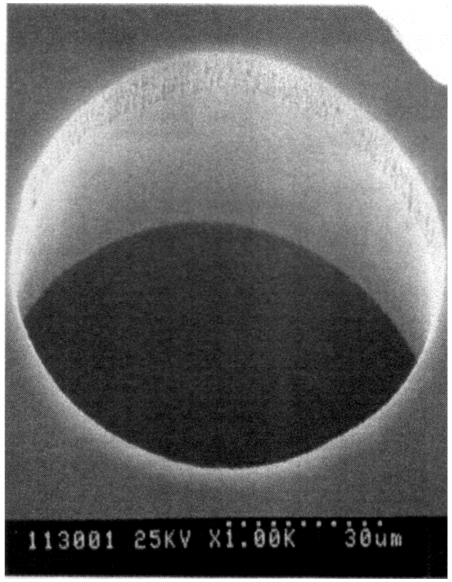


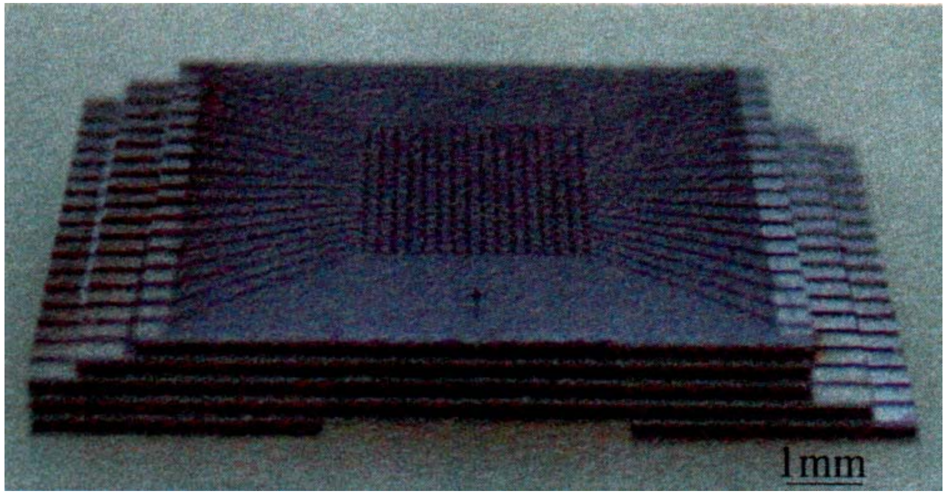
Fowler-Nordheim plot with and without laser irradiation

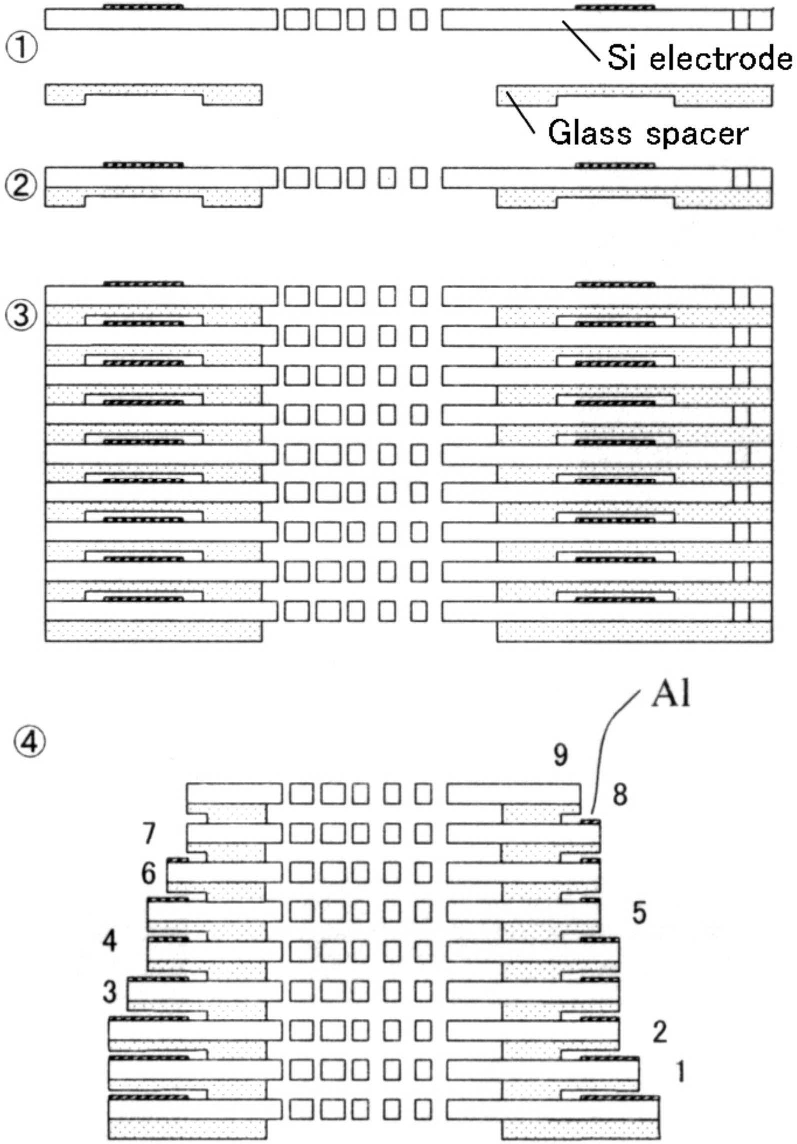


(E. Tomono, H. Miyashita, T. Ono and M. Esashi, APCOT 2010)



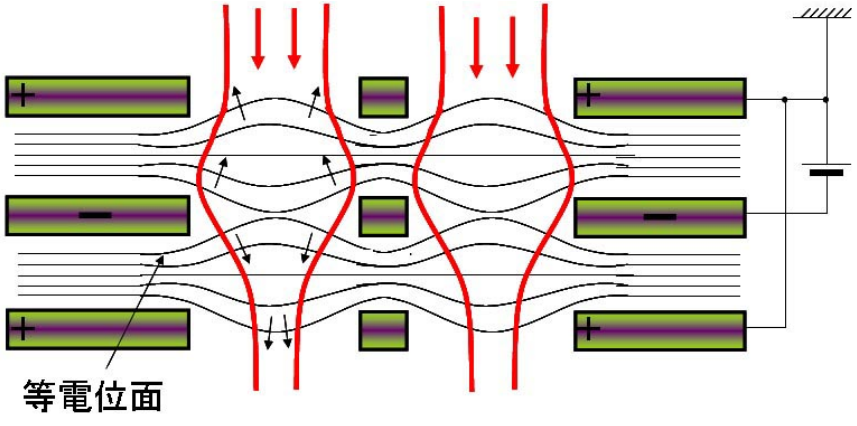




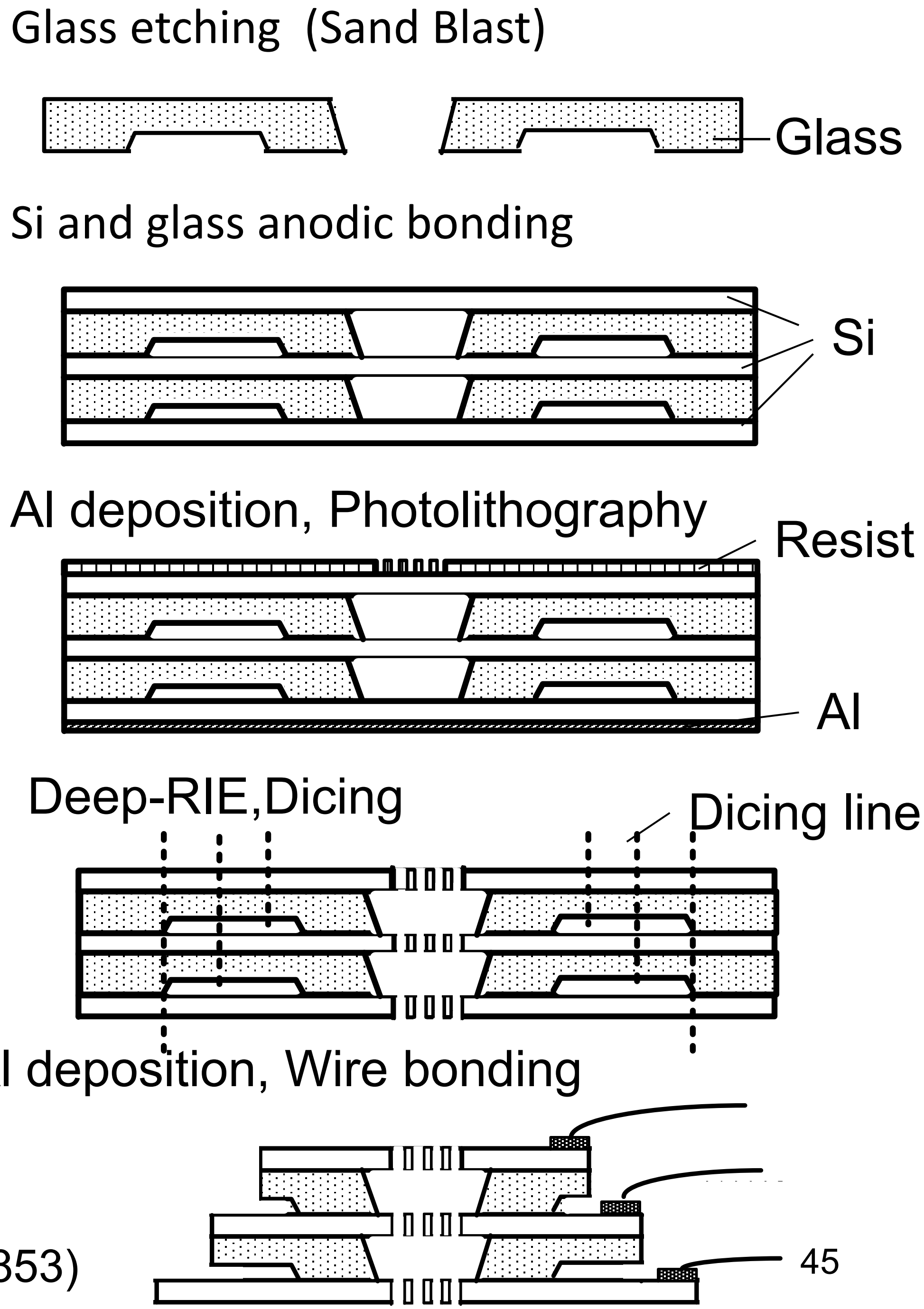


Fabrication process

Correction Lens Array (F.Hirose (Cannon) 2003)

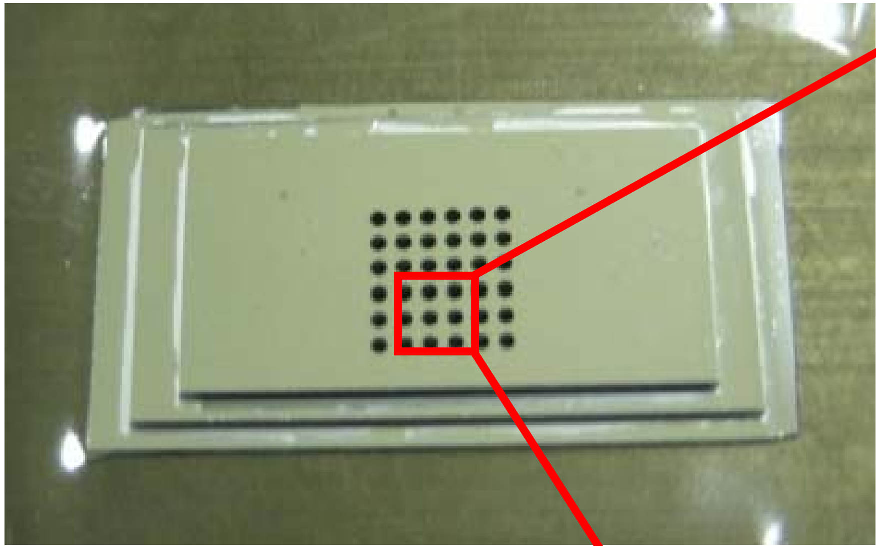


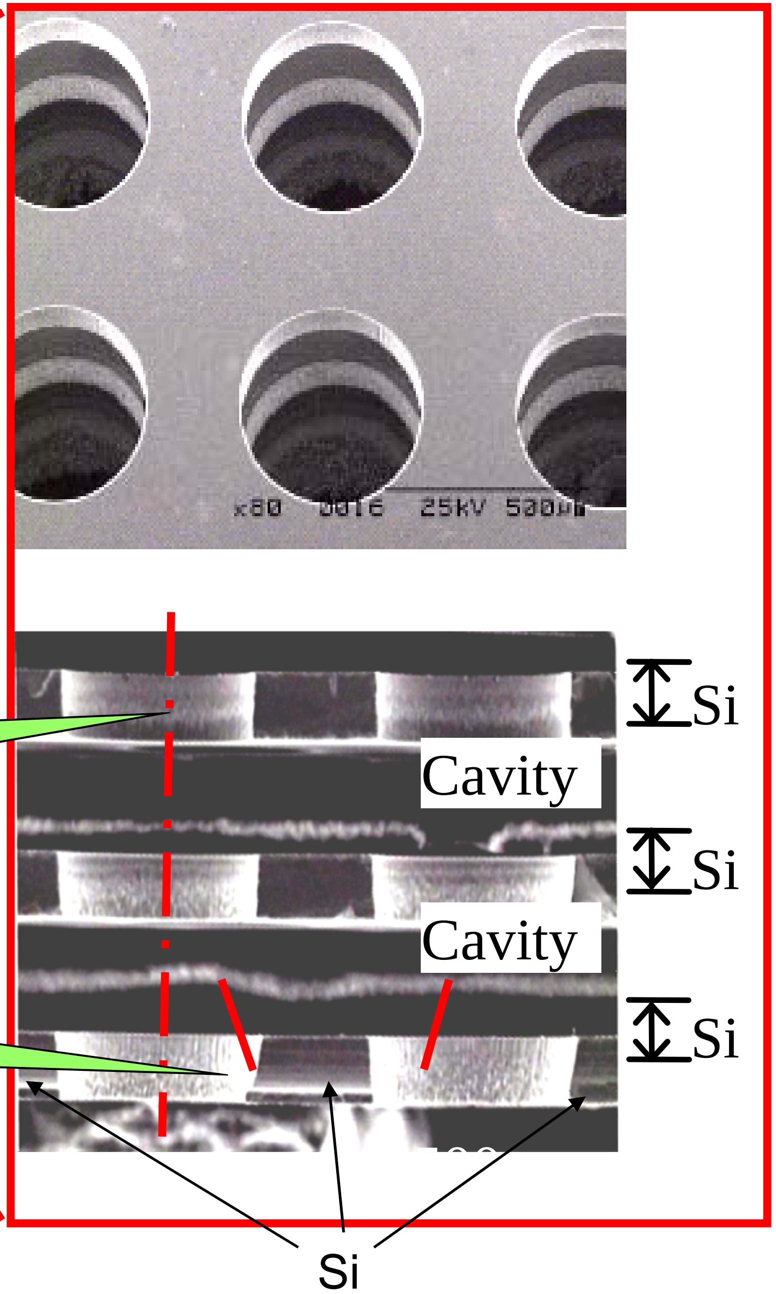
原理



Principle and fabrication process of electrostatic lens

(E.Tomono,Transducers 2009 (2009) p.853)





All electrodes
are exactly aligned.

The hall of third layers
have taper angles.

Fabricated electrostatic lens

(E.Tomono,Transducers 2009 (2009) p.853)