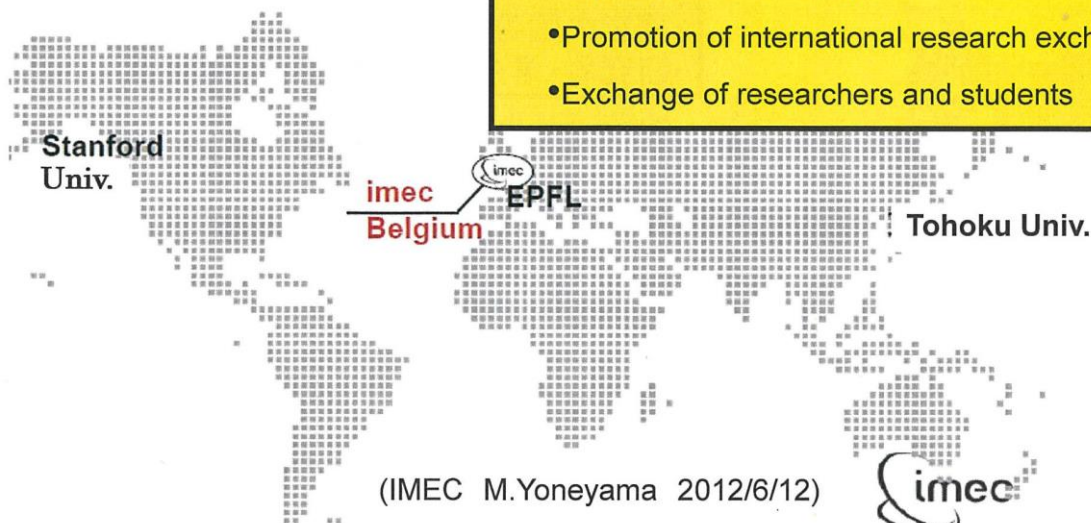


Strategic Partner

- One university from each region,
Japan, USA and Europe
- Promotion of international research exchange
- Exchange of researchers and students



← Hiroshi Kazui (Director, Tohoku Univ.) and Luc Van Den Hove (IMEC president)

Signing ceremony
(2012/6/11) →



Joint Seminar in IMEC
(2012/6/21)
Alternative annual meeting in IMEC and Tohoku University

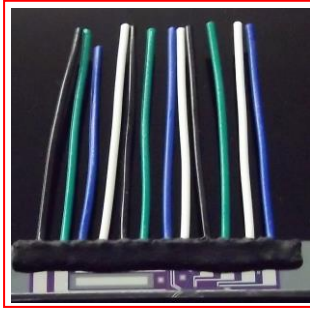
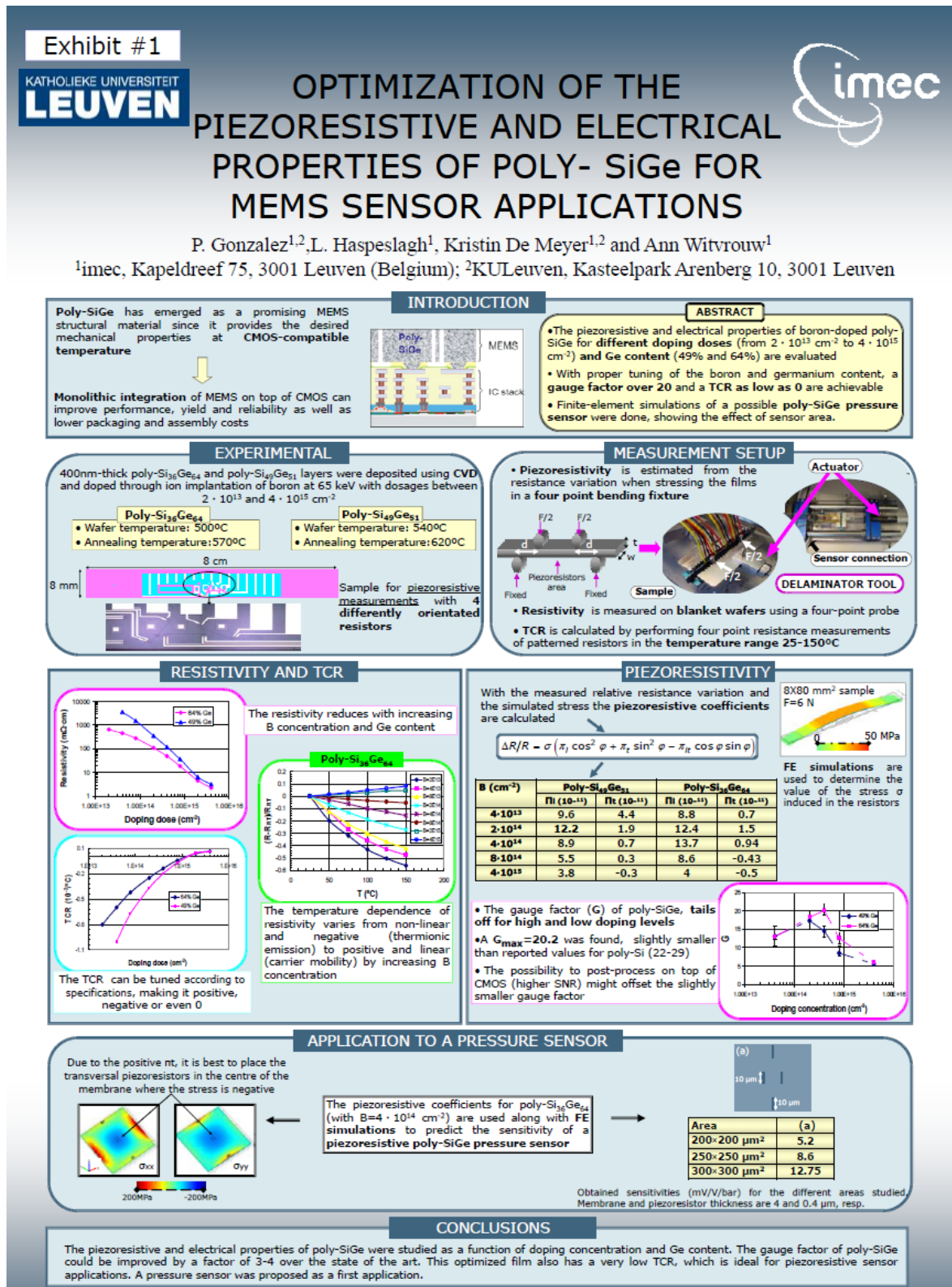


Exhibit #1: Sample to determine the piezoresistivity of a poly-SiGe layer by measuring the resistance changes during 4-point bending tests.



ISSCC 2005 / SESSION 4 / TD: MIXED-DOMAIN SYSTEMS

4.7 Processing of MEMS Gyroscopes on Top of CMOS ICs

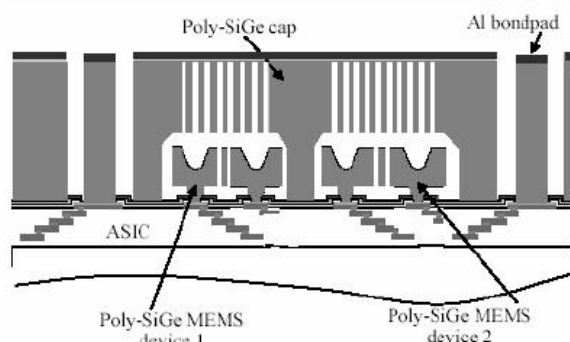
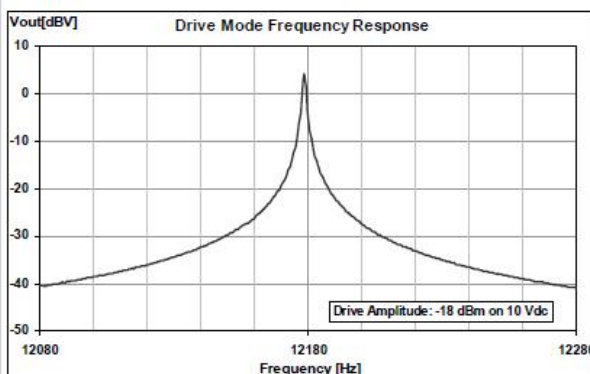
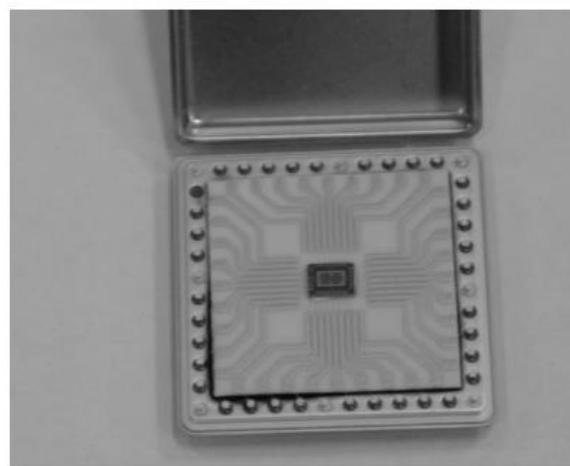
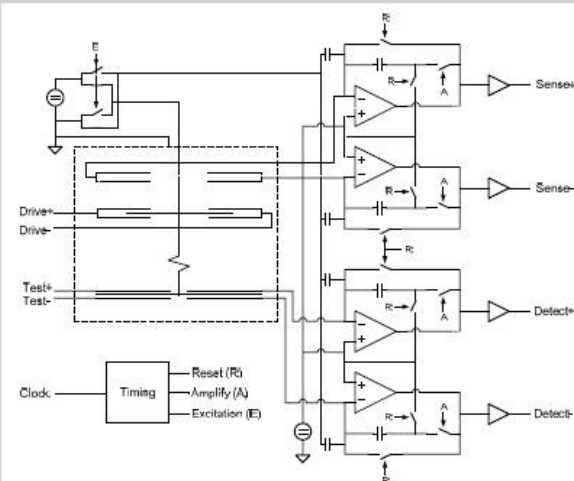
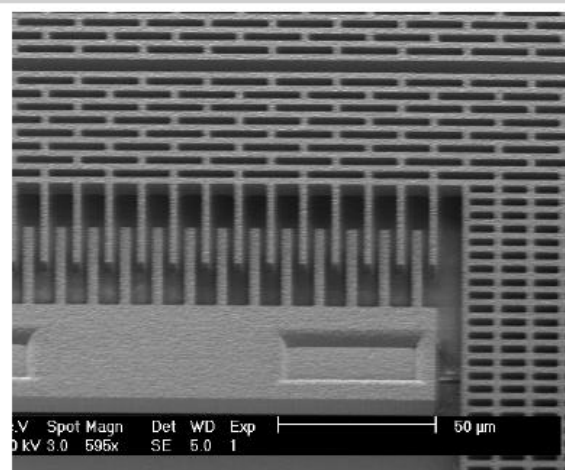
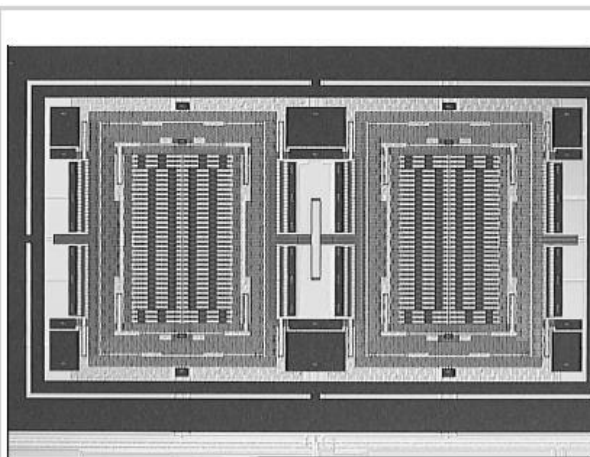
A. Witvrouw¹, A. Mehta¹, A. Verbist¹, B. Du Bois¹, S. Van Aerde², J. Ramos-Martos³, J. Ceballos³, A. Ragel³, J. M. Mora³, M.A. Lagos³, A. Arias³, J. M. Hinojosa³, J. Spengler⁴, C. Leinenbach⁵, T. Fuchs⁵, S. Kronmüller⁵

¹IMEC, Leuven, Belgium, ²ASM, Leuven, Belgium, ³IMSE-CNM, Sevilla, Spain,

⁴Philips, Böblingen, Germany, ⁵Bosch, Gerlingen-Schillerhöhe, Germany



Exhibit #2: First poly-SiGe above-CMOS integrated gyroscope. The CMOS technology used is a standard 0.35 μm technology with 5 interconnect levels.



H4 SiGe micro-mirror array on CMOS IC

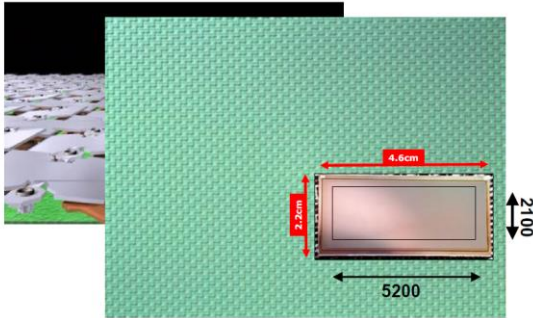
Ann Witvrouw

Exhibit #3: 11 megapixel micro-mirror array with 8 μm pitch made in poly-SiGe above standard 0.18 μm analog-CMOS wafers fabricated by NXP, featuring 6 interconnect levels.



11MPixel micro-mirror array

- To be used as SLM (Spatial Light modulator)

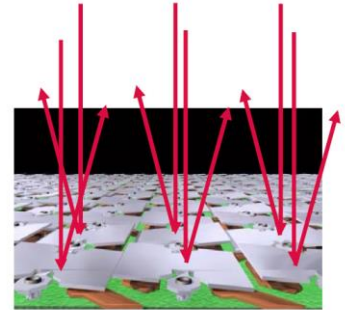


Project together with ASML, Bruco, NXP, Philips Appl. Tech.

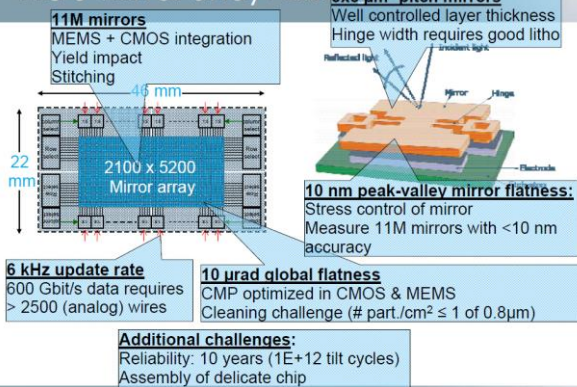
11MPixel micro-mirror array: application

Spatial Light Modulator:

- Light is deflected by each mirror to create image
- Applications: video projection, mask writing, maskless imaging



Micro-mirror array: Challenges



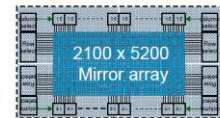
Micro-mirrors: State-of-the-art

TI DLP Discovery 4000:
1920x1080 (2M)
Digital
Mirror Pitch 10.8 μm
Mirror Area 21 x 12 mm² (2.5 cm²)
<www.dlp.com

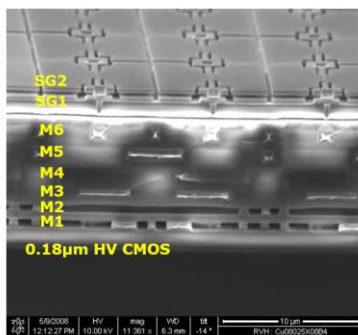
Fraunhofer SLM:
2048x512 (1M)
Analog
Mirror Pitch 16 μm
Mirror Area 33 x 8 mm² (2.6 cm²)
<www.ipms.fraunhofer.de

This work:

5200x2100 (11M)
Analog
Mirror Pitch 8 μm
Mirror area 42 x 17 mm² (7 cm²)



Micro-mirrors: processing

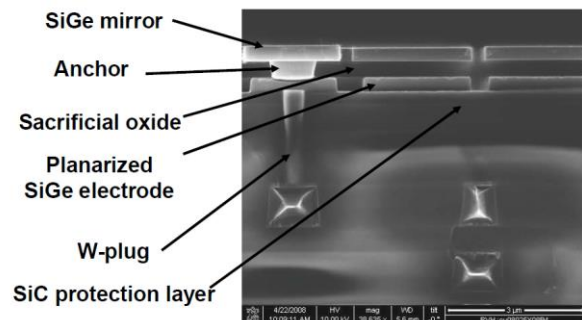


SiGe is chosen to achieve required mirror specs including reliability at CMOS-compatible T

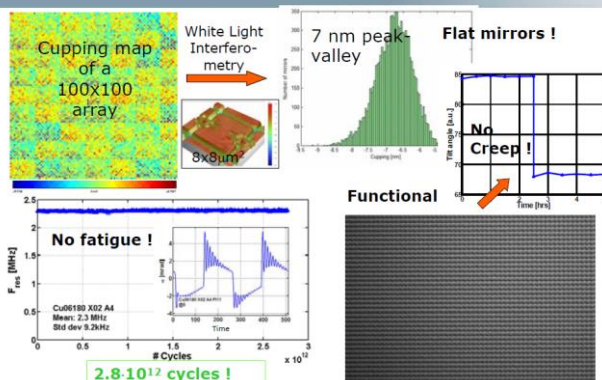
SiGe-based micro-mirror module
Planarised interface
0.18 μm analog CMOS with 6 metal levels (from NXP)

< L. Haspeslagh et al., Proc IEDM 2008

Micro-mirrors: processing



Micro-mirrors: functional & reliability analysis



Micro-mirrors: packaging and testing

Mirror performance after packaging
123648 mirrors tested

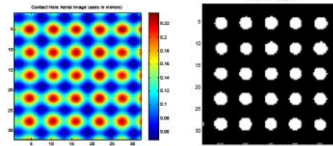
| Item | Specification | Results |
|-----------------|---------------|---------|
| Good Mirrors % | / | 99.5 % |
| Mean Cupping | < 10 nm | 5.4 nm |
| Residual Piston | < 1nm | < 1 nm |

Direct imaging:
3 mirror contact holes



Packaging and assembly
A. Witvrouw et al. Proc. MEMS09

Imaging results: J. Lauria et al, Microel. Eng. 86, 569-572 (2009)



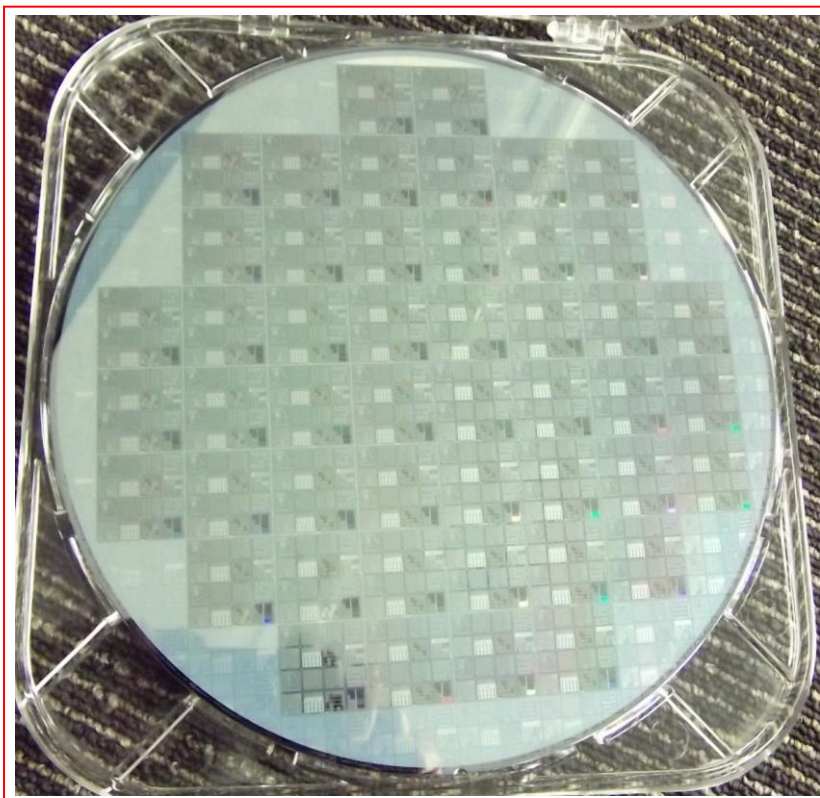


Exhibit #4: Poly-SiGe MEMS MultiProject Wafer (MPW) from the first SiGeMEMS MPW run organized by Europractice in 2011.



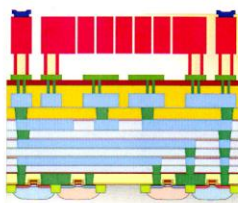
imec CMORE SiGeMEMS MPW

EUROPRACTICE IC Service offers Multi-Project Wafer Services in imec's CMORE SiGeMEMS standalone and SiGeMEMS/CMOS integrated technology:

Imec's **CMORE Silicon Germanium MEMS** platform technology, referred to as **SiGeMEMS**, is developed to enable monolithic integration of CMOS and MEMS. Systems integrating MEMS devices with the driving and readout electronics on the same die lead to better performances in terms of signal to noise ratio through reduced interconnect parasitic resistance and capacitance, allow for smaller die size and package, and also for lower power consumption. SiGeMEMS is based on a MEMS-last approach which allows state-of-the-art CMOS foundries to be employed.

Technology

The **SiGeMEMS** process, belonging to imec's CMORE service platform, is very versatile. Thanks to its flexible and modular approach, allowing application-specific tuning and optimization, it addresses a large number of applications like gyro's, switches, microphones, uspeakers, CMUTs, T-sensors, P-sensors, ... and array type devices like μmirrors, probe-based memories, and arrays for μfluidics and upower generation...



EUROPRACTICE now offers a fixed baseline **SiGeMEMS** process in a Multi-Project Wafer Service. This unique baseline process consists of MEMS structures defined by an electrode layer and a 4μm-thick SiGe-mechanical layer on top of a TSMC 0.18μm CMOS wafer. Nanogaps of 500nm will allow fabrication of extremely small features. A standalone MEMS version, identical but processed on a wafer with a single metal layer, will be available for initial prototyping.

Europractice-imec SiGeMEMS MPW runs in 2012

| Imec CMORE | 2012 | | | | | | | | | | | |
|--|------|---|---|---|---|----|---|---|---|---|------------------|---|
| | J | F | M | A | M | J | J | A | S | O | N | D |
| SiGeMEMS MEMS-only | | | | | | | | | | | 20 | |
| SiGeMEMS/TSMC 0.18μm CMOS (CVD18LD 1.8/3.3/2V) | | | | | | 10 | | | | | 25 ¹⁾ | |

Note: 1) This run is preliminary and can be updated during 2012

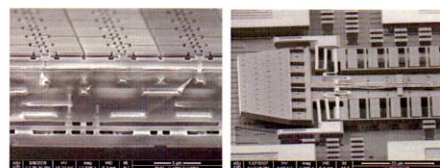
Price

| Technology Version | Standard Price | EU-Discounted Price |
|--------------------|----------------|---------------------|
| MEMS-only | 4250 € | 4000 € |
| CMOS integrated | 28500 € | 27000 € |

EU-Discounted Price only applies to EUROPRACTICE registered (who paid their annual full membership fee) Academic and Research Members from all 27 EU countries and Norway, Iceland, Liechtenstein, Israel, Croatia, Serbia, Macedonia, Albania, Montenegro, Bosnia-Herzegovina, Switzerland, Turkey who submit designs for educational or publicly funded research use only.

Standard Price normal price for universities and research institutes not belonging to previous category. (Companies should contact imec CMORE at www.imec.be/cmcore to take advantage of additional extensions and services)

Prices and conditions may change at any time without prior notice



For more information: epmms@imec.be

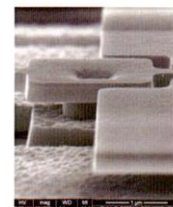
www.europractice-ic.com



imec CMORE SiGeMEMS MPW

Principle

Imec's CMORE **SiGeMEMS** technology offered through the **EUROPRACTICE IC** MPW service is aimed at creating, characterizing and evaluating test structures prior to further specific development and production projects. By gathering the designs of multiple customers on the same masks set, MPWs allow to fabricate test structures and prototypes of devices at a low cost.



Advantages of SiGeMEMS

Monolithic integration with IC :

- Very compact
- Best solution for applications that are very sensitive to parasitics
- High intrinsic system reliability: less components, less interconnections.

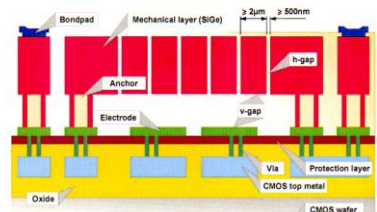
MEMS last above CMOS :

- Most flexible with respect to choice of CMOS technology
- Extremely well suited for MEMS array applications
 - very high-density and massively parallel interconnections possible
 - large arrays of MEMS (e.g. μmirror arrays)

Poly-SiGe :

- High performance: low parasitics
- Good mechanical properties & reliability
 - better than Al: higher strength and Q factor
 - better than Al: less creep and fatigue

Summary of SiGeMEMS main features and dimensions



General conditions :

EUROPRACTICE **SiGeMEMS** MPW Service is accessible for universities and research institutes. (EUROPRACTICE registered members) → more info at www.europractice-ic.com

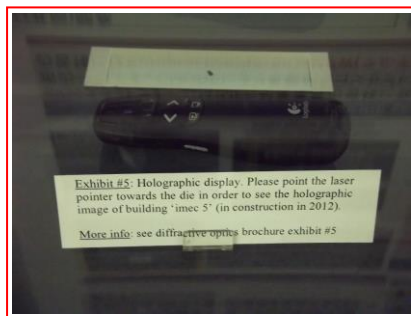
Companies can have additional extensions to take advantage of the versatile, flexible and modular technology:

- Variable layer thicknesses
- Application-specific optimization of layer & material properties
- Application-specific functional add-on layers

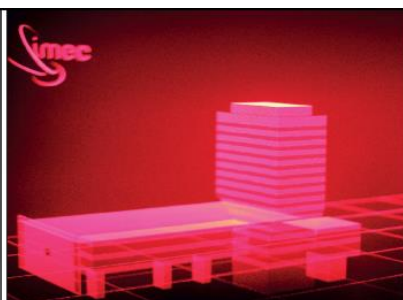
Companies should contact imec CMORE at www.imec.be/cmcore

For more information: epmms@imec.be

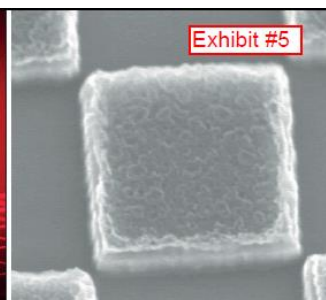
www.europractice-ic.com



Set-up for holographic display technology.



Holographic image demonstrator.



SEM-image of sub-wavelength binary holographic pixel.

DIGITAL DIFFRACTIVE OPTICS PATH TO HIGH-QUALITY HOLOGRAPHIC DISPLAYS

Vision

Imagine having a meeting. You and your guests sit around the table arguing, discussing or presenting data. Just like any meeting you have today, only for one detail: some of the people around the table are 3D images – dynamic holograms – of people sitting in an office thousands of miles away. You will look them in the eye, feel their hesitations, and see their body language. Unlike with today's displays, you won't miss a cue.

Holographic visualization promises to offer a natural 3D experience for multiple viewers, without the undesirable side-effects of current 3D stereoscopic visualization (uncomfortable glasses, strained eyes, fatiguing experience). Imec's vision is to design the ultimate 3D display: a holographic display with wide viewing angle and a high-definition visual experience.

Challenges

Building a high-quality, real-time holographic display requires several breakthroughs from today's holographic prototypes. The challenges are threefold:

- To achieve high image quality, millions of light-diffracting elements are needed. These must all be individually controlled.
- To achieve a wide viewing angle, the light-diffracting elements should be sized close to or below the wavelength of the visible light, i.e. as small as a few hundred nanometers.
- To achieve real-time imaging, massive computing power is needed.

Technology

Imec is scaling its MEMS technology to meet these challenging demands. Our prototypes show promising results, setting the path to high-quality displays.

Imec aims for system-level solutions utilizing a unique combination of its multi-disciplinary teams with strong competences in:

- Advanced lithography
- Silicon processing
- SiGe MEMS processing platform
- MEMS design & prototyping
- Computational holography
- Holographic (lens-less) imaging
- Sub-wavelength diffractive optics
- Embedded system design
- Parallel computing platforms

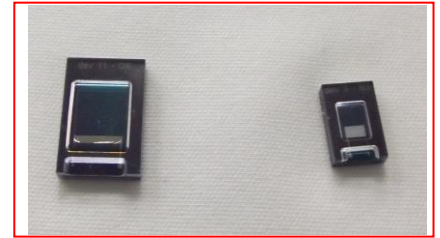
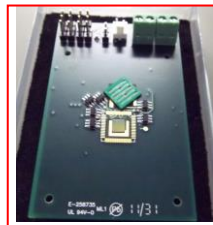
Our longer-term goal is to create a display system for computer-generated holography with billions of sub-wavelength diffractive elements, delivering high-definition 3D visual experience.



www.imec.be



Imec, The Netherlands



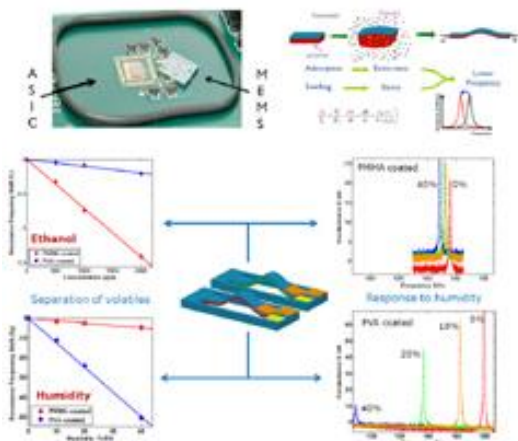
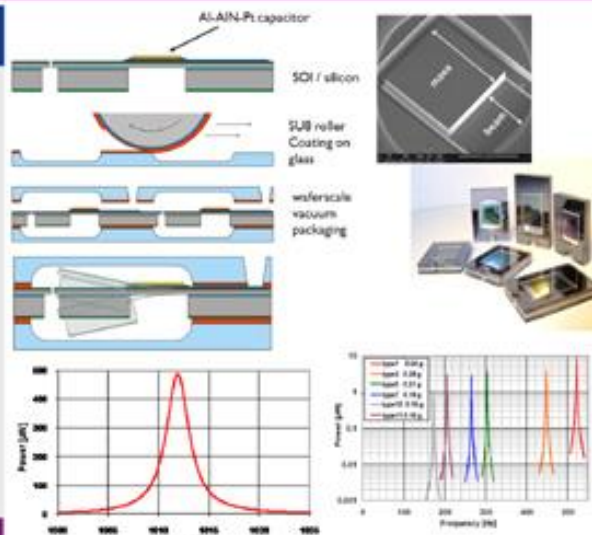
MEMS FOR ENERGY HARVESTERS & ELECTRONIC NOSE

Background

Wireless sensor nodes are able to operate autonomously, for extended periods of time, provided they are equipped with Ultra Low Power components, and their energy is supplied by energy harvesters. For both the sensors as well as the harvesters, MEMS fabrication by bulk machining is an enabling technology.

Energy Harvesting

The **Piezo Vibration Harvester** is processed on SOI wafers. An Al-AIN-Pt is deposited and subsequently the beam and mass are defined using DRIE. The devices are vacuum packaged with two glass wafers with a cavity. Roller coating is used for this process. Several devices have been designed, each with their own resonance frequency (between 200Hz and 1 kHz). The maximum power output has been $489\mu\text{W}$ at an input acceleration of $4.5g$.



Ultra Low Power Electronic Nose

MEMS cantilevers are traditionally used for mass based (bio-)sensing as the resonance frequency shifts when molecules adsorb.

Here, an electronic nose based on the response of an array of MEMS resonators is developed, where each resonator is coated with a different polymer and thus reacts differently when exposed to the environment. This approach, where swelling of the polymers gives a stress induced resonance shift, is significantly more sensitive ($\sim 300\times$ compared to mass based sensing), thus enabling detection of low-mass volatiles with a scalable MEMS array. Additionally, a dedicated ASIC is developed that actuates the device through a piezo-electric patch, and tracks the resonance frequency.