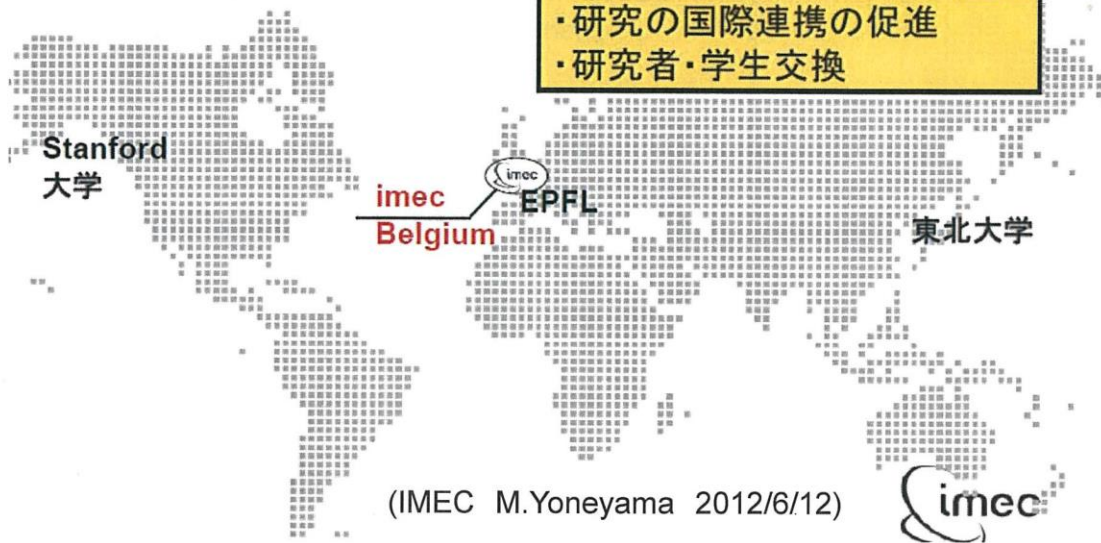


Strategic Partner
東北大学・Stanford大学・EPFL

- ・日・米・欧から1大学ずつ選定
- ・研究の国際連携の促進
- ・研究者・学生交換



(IMEC M.Yoneyama 2012/6/12)



← 数井 東北大理事と
Luc Van Den Hove
IMEC社長

協 定 調 印 式
(2012/6/11)中央は
ベルギーのフィリッ
プ皇太子 →



IMEC での
共同セミナー
(2012/6/21)
毎年交互開
催

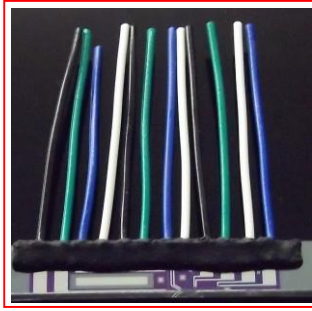


Exhibit #1: Sample to determine the piezoresistivity of a poly-SiGe layer by measuring the resistance changes during 4-point bending tests.

Exhibit #1

KATHOLIEKE UNIVERSITEIT
LEUVEN

OPTIMIZATION OF THE PIEZORESISTIVE AND ELECTRICAL PROPERTIES OF POLY- SiGe FOR MEMS SENSOR APPLICATIONS



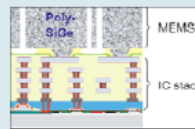
P. Gonzalez^{1,2}, L. Haspelslagh¹, Kristin De Meyer^{1,2} and Ann Witvrouw¹

¹imec, Kapeldreef 75, 3001 Leuven (Belgium); ²KULeuven, Kasteelpark Arenberg 10, 3001 Leuven

Poly-SiGe has emerged as a promising MEMS structural material since it provides the desired mechanical properties at CMOS-compatible temperature

Monolithic integration of MEMS on top of CMOS can improve performance, yield and reliability as well as lower packaging and assembly costs

INTRODUCTION



ABSTRACT

- The piezoresistive and electrical properties of boron-doped poly-SiGe for different doping doses (from $2 \cdot 10^{13} \text{ cm}^{-2}$ to $4 \cdot 10^{15} \text{ cm}^{-2}$) and Ge content (49% and 64%) are evaluated
- With proper tuning of the boron and germanium content, a gauge factor over 20 and a TCR as low as 0 are achievable
- Finite-element simulations of a possible poly-SiGe pressure sensor were done, showing the effect of sensor area.

EXPERIMENTAL

400nm-thick poly-Si₃₅Ge₆₄ and poly-Si₄₉Ge₅₁ layers were deposited using CVD and doped through ion implantation of boron at 65 keV with dosages between $2 \cdot 10^{13}$ and $4 \cdot 10^{15} \text{ cm}^{-2}$

- Poly-Si₃₅Ge₆₄
 - Wafer temperature: 500°C
 - Annealing temperature: 570°C

- Poly-Si₄₉Ge₅₁
 - Wafer temperature: 540°C
 - Annealing temperature: 620°C



Sample for piezoresistive measurements with 4 differently orientated resistors

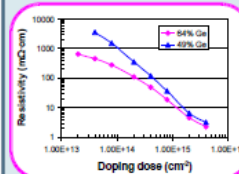
MEASUREMENT SETUP

- Piezoresistivity is estimated from the resistance variation when stressing the films in a four point bending fixture

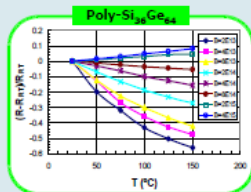


- Resistivity is measured on blanket wafers using a four-point probe
- TCR is calculated by performing four point resistance measurements of patterned resistors in the temperature range 25-150°C

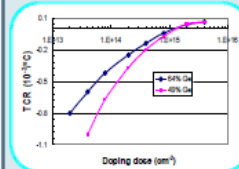
RESISTIVITY AND TCR



The resistivity reduces with increasing B concentration and Ge content



The temperature dependence of resistivity varies from non-linear and negative (thermionic emission) to positive and linear (carrier mobility) by increasing B concentration



The TCR can be tuned according to specifications, making it positive, negative or even 0

PIEZORESISTIVITY

With the measured relative resistance variation and the simulated stress the piezoresistive coefficients are calculated

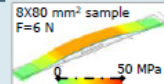
$$\Delta R/R = \sigma (\pi_l \cos^2 \varphi + \pi_t \sin^2 \varphi - \pi_{lt} \cos \varphi \sin \varphi)$$

B (cm ⁻²)	Poly-Si ₃₅ Ge ₆₄		Poly-Si ₄₉ Ge ₅₁	
	$\pi_l (10^{-11})$	$\pi_t (10^{-11})$	$\pi_l (10^{-11})$	$\pi_t (10^{-11})$
$4 \cdot 10^{13}$	9.6	4.4	8.8	0.7
$2 \cdot 10^{14}$	12.2	1.9	12.4	1.5
$4 \cdot 10^{14}$	8.9	0.7	13.7	0.94
$8 \cdot 10^{14}$	5.5	0.3	8.6	-0.43
$4 \cdot 10^{15}$	3.8	-0.3	4	-0.5

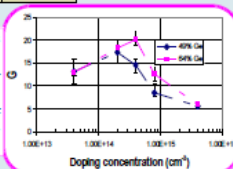
- The gauge factor (G) of poly-SiGe, tails off for high and low doping levels

- A $G_{\max} = 20.2$ was found, slightly smaller than reported values for poly-Si (22-29)

- The possibility to post-process on top of CMOS (higher SNR) might offset the slightly smaller gauge factor

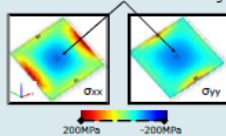


FE simulations are used to determine the value of the stress σ induced in the resistors

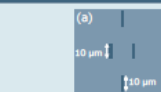


APPLICATION TO A PRESSURE SENSOR

Due to the positive nt, it is best to place the transversal piezoresistors in the centre of the membrane where the stress is negative



The piezoresistive coefficients for poly-Si₃₅Ge₆₄ (with $B = 4 \cdot 10^{14} \text{ cm}^{-2}$) are used along with FE simulations to predict the sensitivity of a piezoresistive poly-SiGe pressure sensor



Area	(a)
200×200 μm ²	5.2
250×250 μm ²	8.6
300×300 μm ²	12.75

Obtained sensitivities (mV/V/bar) for the different areas studied. Membrane and piezoresistor thickness are 4 and 0.4 μm, resp.

CONCLUSIONS

The piezoresistive and electrical properties of poly-SiGe were studied as a function of doping concentration and Ge content. The gauge factor of poly-SiGe could be improved by a factor of 3-4 over the state of the art. This optimized film also has a very low TCR, which is ideal for piezoresistive sensor applications. A pressure sensor was proposed as a first application.

4.7 Processing of MEMS Gyroscopes on Top of CMOS ICs

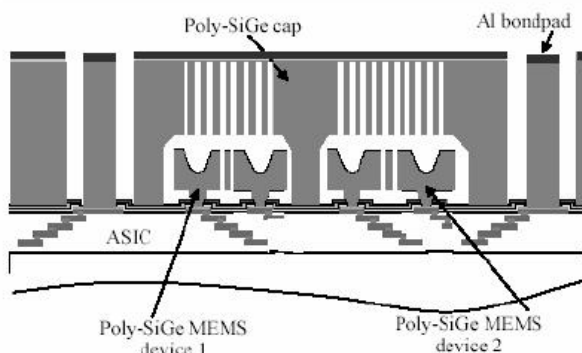
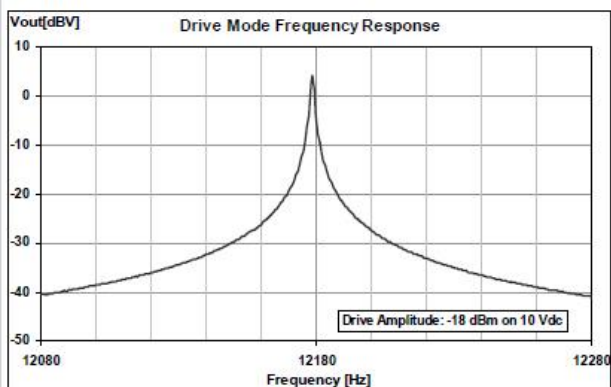
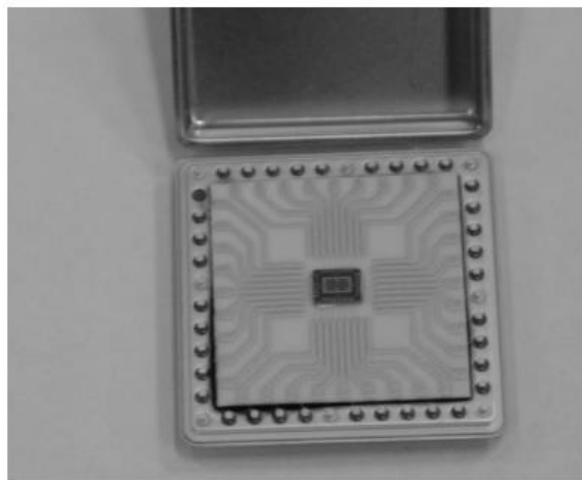
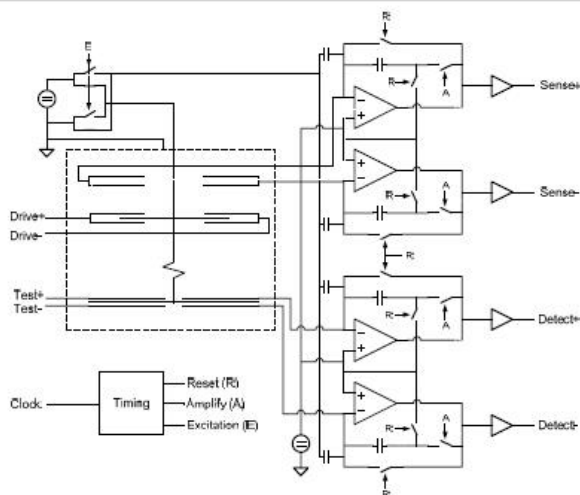
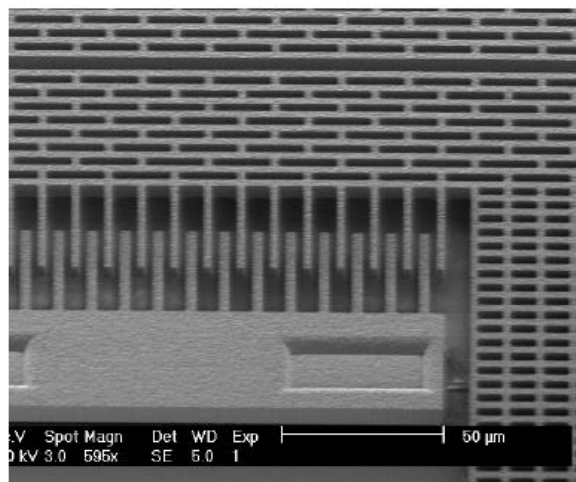
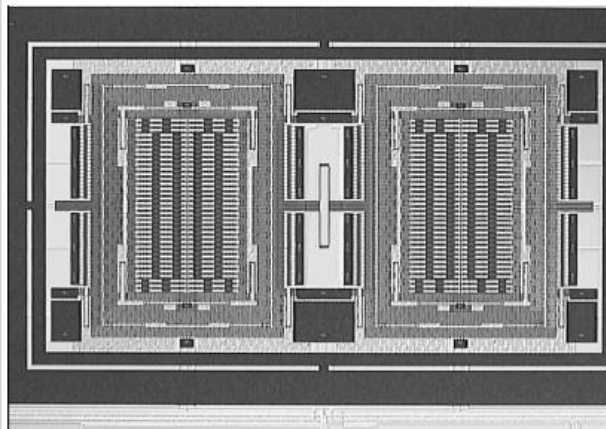
A. Witvrouw¹, A. Mehta¹, A. Verbist¹, B. Du Bois¹, S. Van Aerde²,
J. Ramos-Martos³, J. Ceballos³, A. Ragel³, J. M. Mora³, M.A. Lagos³, A. Arias³,
J. M. Hinojosa³, J. Spengler⁴, C. Leinenbach⁵, T. Fuchs⁵, S. Kronmüller⁵

¹IMEC, Leuven, Belgium, ²ASM, Leuven, Belgium, ³IMSE-CNM, Sevilla, Spain,

⁴Philips, Böblingen, Germany, ⁵Bosch, Gerlingen-Schillerhöhe, Germany



Exhibit #2: First poly-SiGe above-CMOS integrated gyroscope. The CMOS technology used is a standard 0.35 μm technology with 5 interconnect levels.



CMOS IC 上 SiGe ミラーアレイ

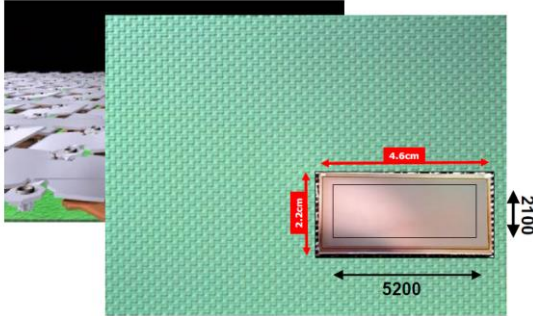
Ann Witvrouw

Exhibit #3: 11 megapixel micro-mirror array with 8 μm pitch made in poly-SiGe above standard 0.18 μm analog-CMOS wafers fabricated by NXP, featuring 6 interconnect levels.



11MPixel micro-mirror array

- To be used as SLM (Spatial Light modulator)

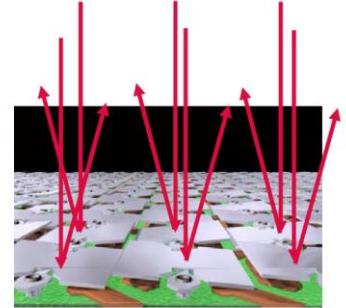


Project together with ASML, Bruco, NXP, Philips Appl. Tech.

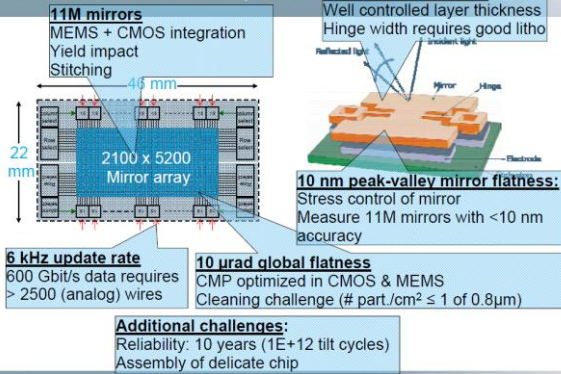
11MPixel micro-mirror array: application

Spatial Light Modulator:

- Light is deflected by each mirror to create image
- Applications: video projection, mask writing, maskless imaging



Micro-mirror array: Challenges

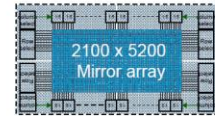


Micro-mirrors: State-of-the art

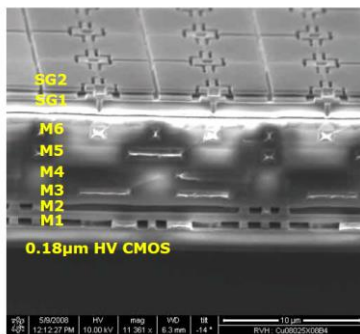


This work:

5200x2100 (11M)
Analog
Mirror Pitch 8 μm
Mirror area 42 x 17 mm²
(7 cm²)



Micro-mirrors: processing

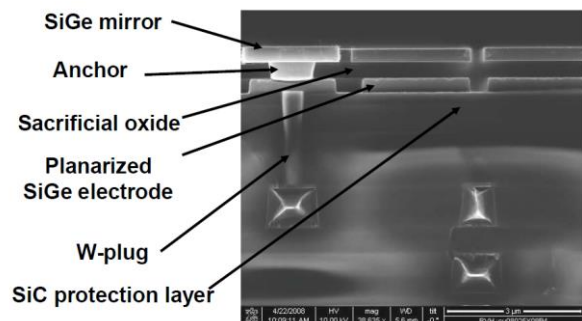


SiGe is chosen to achieve required mirror specs including reliability at CMOS-compatible T

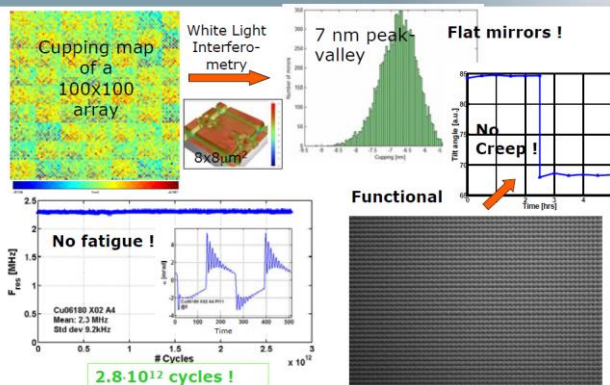
SiGe-based micro-mirror module
Planarised interface
0.18 μm analog CMOS with 6 metal levels (from NXP)

< L. Haspeslagh et al., Proc. IEDM 2008

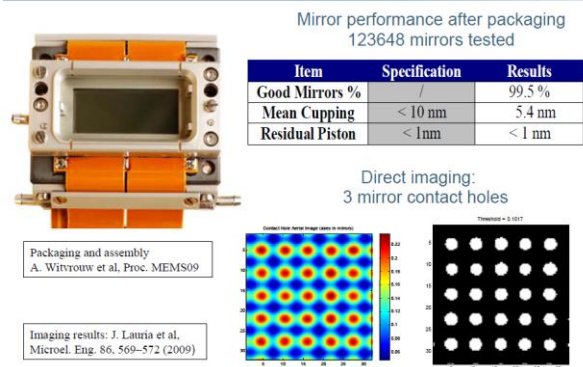
Micro-mirrors: processing



Micro-mirrors: functional & reliability analysis

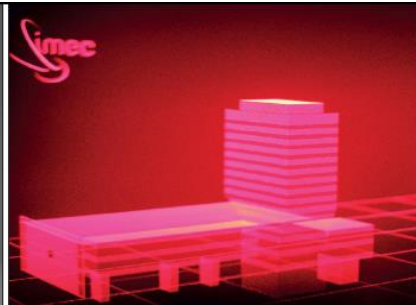


Micro-mirrors: packaging and testing

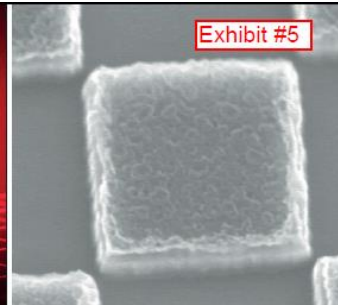




Set-up for holographic display technology.



Holographic image demonstrator.



SEM-image of sub-wavelength binary holographic pixel.

DIGITAL DIFFRACTIVE OPTICS PATH TO HIGH-QUALITY HOLOGRAPHIC DISPLAYS

Vision

Imagine having a meeting. You and your guests sit around the table arguing, discussing or presenting data. Just like any meeting you have today, only for one detail: some of the people around the table are 3D images – dynamic holograms – of people sitting in an office thousands of miles away. You will look them in the eye, feel their hesitations, and see their body language. Unlike with today's displays, you won't miss a cue.

Holographic visualization promises to offer a natural 3D experience for multiple viewers, without the undesirable side-effects of current 3D stereoscopic visualization (uncomfortable glasses, strained eyes, fatiguing experience). Imec's vision is to design the ultimate 3D display: a holographic display with wide viewing angle and a high-definition visual experience.

Challenges

Building a high-quality, real-time holographic display requires several breakthroughs from today's holographic prototypes. The challenges are threefold:

- To achieve high image quality, millions of light-diffracting elements are needed. These must all be individually controlled.
- To achieve a wide viewing angle, the light-diffracting elements should be sized close to or below the wavelength of the visible light, i.e. as small as a few hundred nanometers.
- To achieve real-time imaging, massive computing power is needed.

Technology

Imec is scaling its MEMS technology to meet these challenging demands. Our prototypes show promising results, setting the path to high-quality displays.

Imec aims for system-level solutions utilizing a unique combination of its multi-disciplinary teams with strong competences in:

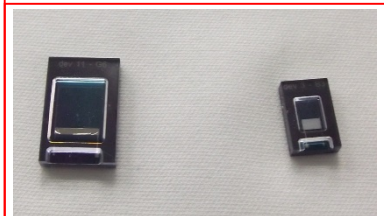
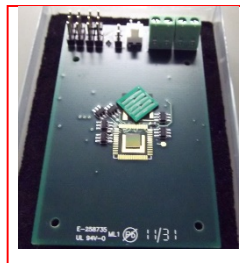
- Advanced lithography
- Silicon processing
- SiGe MEMS processing platform
- MEMS design & prototyping
- Computational holography
- Holographic (lens-less) imaging
- Sub-wavelength diffractive optics
- Embedded system design
- Parallel computing platforms

Our longer-term goal is to create a display system for computer-generated holography with billions of sub-wavelength diffractive elements, delivering high-definition 3D visual experience.



www.imec.be

H7 エネルギーハーベスタ用 MEMS と電子嗅覚



エネルギーハーベスタ用 MEMS と電子嗅覚

Imec, The Netherlands

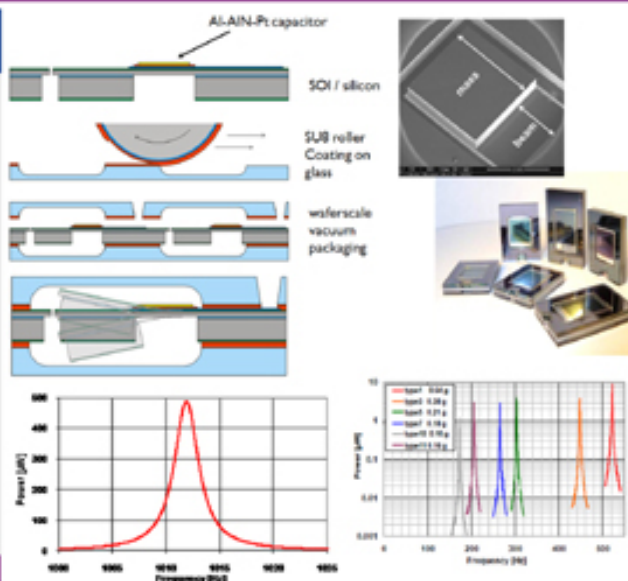
Background

Wireless sensor nodes are able to operate autonomously, for extended periods of time, provided they are equipped with Ultra Low Power components, and their energy is supplied by energy harvesters. For both the sensors as well as the harvesters, MEMS fabrication by bulk machining is an enabling technology.

た
ハ

Energy Harvesting

ピエゾ電気による振動発電デバイスは SOI ウェハに作られます。Al-AIN-Pt を堆積した後、DRIE (深い反応性イオンエッチング) によって梁や錘を形成しています。2 枚のガラスウェハで空洞内に真空封止されていますが、この封止にはローラーによるコーティング法を用います。200Hz から 1KHz の異なる共振周波数を持つ複数のものが設計されており、得られた最大電力は 4.5G の加速度的場合 489 μ W です。



Ultra Low Power Electronic Nose

MEMS 片持ち梁における分子吸着による共振周波数の変化を用いた、質量変化型の(バイオ)センシングが今まで用いられてきました。

IMEC では MEMS 共振子アレイの共振周波数変化を用いた電子嗅覚を開発しました。これはそれぞれの共振子に異なる種類の高分子膜を付けておき、環境中でそれぞれが異なる応答をすることを利用します。この方法では高分子膜が気体を吸着したときに応力変化を生じて共振周波数が変わります。これは質量変化によるものより 300 倍程高感度で、また MEMS アレイの微細化によって微量の気体が検出できます。このための ASIC 回路も作られて、センサデバイスのピエゾ駆動や、共振周波数に追従することを可能にしています。

